DESCRIPTION

174S-04F is a design which includes ESD rated diode arrays to protect high-speed data interfaces. The 174S-04F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), Lightning, and Cable Discharge Event (CDE).

174S-04F is a unique design which includes ESD rated, ultra-low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or to ground line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and on the I/O line, which is protecting any downstream components.

174S-04F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ± 8kV contact discharge).

174S-04F is available in a DFN10 package.

FEATURES

- ESD protection for super speed differential signaling (above 10Gb/s) channels
- Protects four I/O lines
- Provide transient protection for each line to
  IEC 61000-4-2 (ESD) ±15kV (air), ±12kV (contact)
  IEC 61000-4-4 (EFT) 30A (5/50ns)
  IEC 61000-4-5 (Lightning) 4A (8/20us)
- For low operating voltage of 1.5V and below
- Ultra-low capacitance: 0.29pF typical
- Fast turn-on and ultra-low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Solid-state silicon-avalanche and active circuit triggering technology
- Green part
- Available in a DFN10 package.

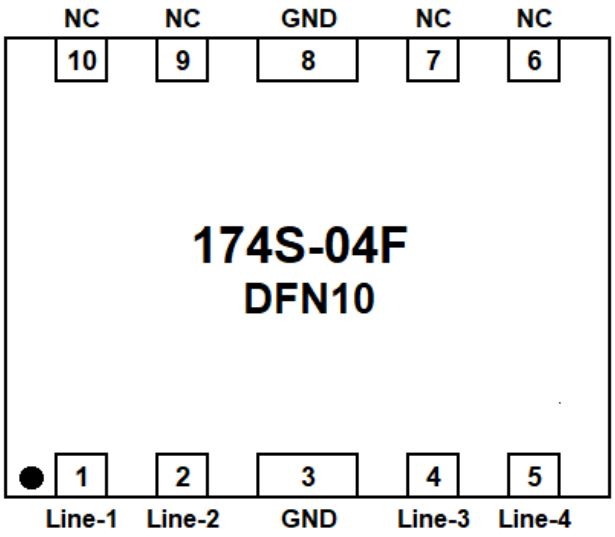
ORDERING INFORMATION

Package Type	Part Number
DFN10	174S-04F
Note	SPQ: 3,000pcs/Reel
AiT provides all RoHS Compliant Products	

APPLICATION

- USB3.1 and USB3.0 interfaces
- Thunderbolt interface
- DisplayPort interface
- SATA and eSATA interface
- V-By-One interface
- Consumer electronics

PIN DESCRIPTION



Top View

Pin #	Symbol	Function
1	Line-1	ESD-Protected Channel
2	Line-2	ESD-Protected Channel
3	GND	Ground
4	Line-3	ESD-Protected Channel
5	Line-4	ESD-Protected Channel
6	NC	No Connection
7	NC	No Connection
8	GND	Ground
9	NC	No Connection
10	NC	No Connection

ABSOLUTE MAXIMUM RATINGS

T_A= 25℃, unless otherwise specified

I_{PP}, Peak Pulse Current (tp =8/20μs)	4A
V_{DC}, Operating Voltage (I/O pin-GND)	1.65V
V_{ESD-1}, ESD per IEC 61000-4-2 (Air)	±15kV
V_{ESD-2}, ESD per IEC 61000-4-2 (Contact)	±12kV
T_{SOL}, Lead Soldering Temperature	260℃ (10 sec.)
T_{OP}, Operating Temperature	-55℃ ~ +125℃
T_{STO}, Storage Temperature	-55℃ ~ +150℃

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

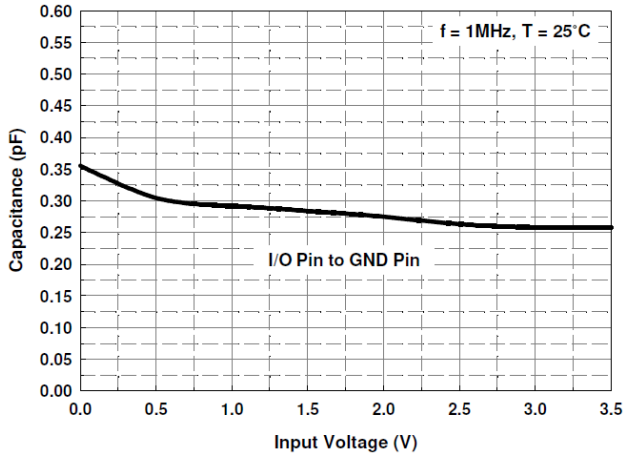
T_A = 25℃, unless otherwise noted

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}	Pin-1,-2,-4,-5 to pin-3,-8, T=25℃.	-	-	1.5	V
Channel Leakage Current	$I_{CH-Leak}$	$V_{Pin-1,-2,-4,-5}$ = 1.5V, $V_{Pin-3,-8}$ = 0V, T=25℃.	-	-	1	μA
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25℃, Pin-1,-2,-4,-5 to pin-3,-8.	5	-	8	V
Forward Voltage	V_F	I_F = 15mA, T=25℃, pin-3,-8 to pin-1,-2,-4,-5.	-	0.9	1.1	V
ESD Clamping Voltage[NOTE1]	V_{CL-ESD}	IEC 61000-4-2 +8kV (I_{TLP} = 16A), Contact mode, T=25℃, any I/O pin to GND.	-	4.3	-	V
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+8kV, T=25℃, Contact mode, any I/O pin to GND.	-	0.19	-	Ω
Channel Input Capacitance	C_{IN}	$V_{pin-3,-8}$ = 0V, V_{IN} = 1.0V, f = 1MHz, T=25℃, any I/O pin to GND.	-	0.29	0.34	pF
Channel to Channel Input Capacitance	C_{CROSS}	$V_{pin-3,-8}$ = 0V, V_{IN} = 1.0V, f = 1MHz, T=25℃, between I/O pins.	-	0.05	0.1	pF

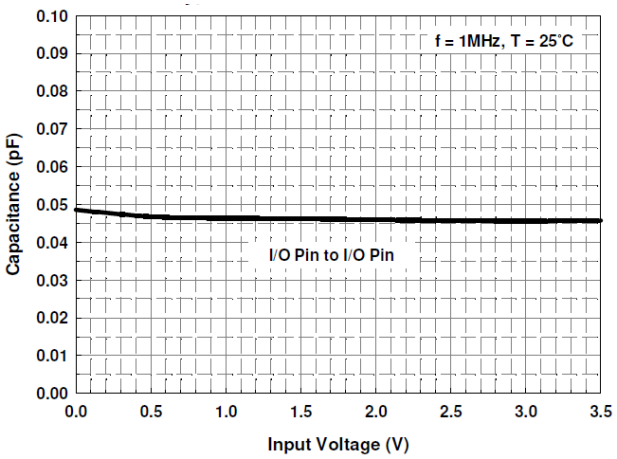
NOTE1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.
TLP conditions: Z_0= 50Ω, t_p= 100ns, t_r= 1ns.

TYPICAL CHARACTERISTICS

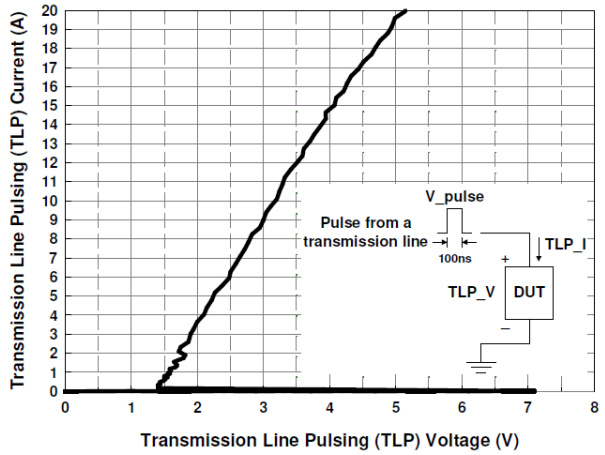
1. Typical Variation of C_{IN} vs. V_{IN}



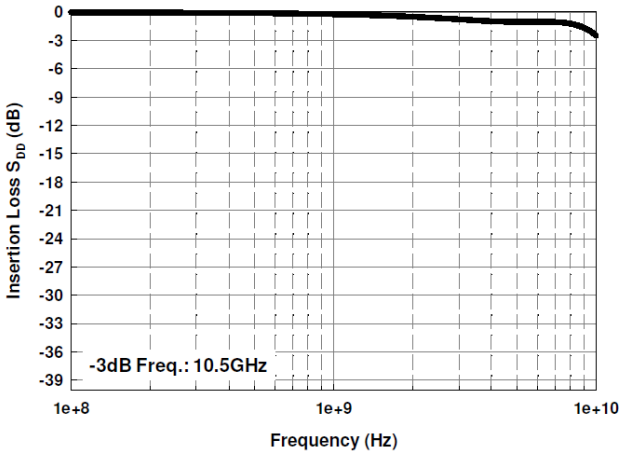
2. Typical Variation of $C_{I/O\text{-}to\text{-}I/O}$ vs. V_{IN}



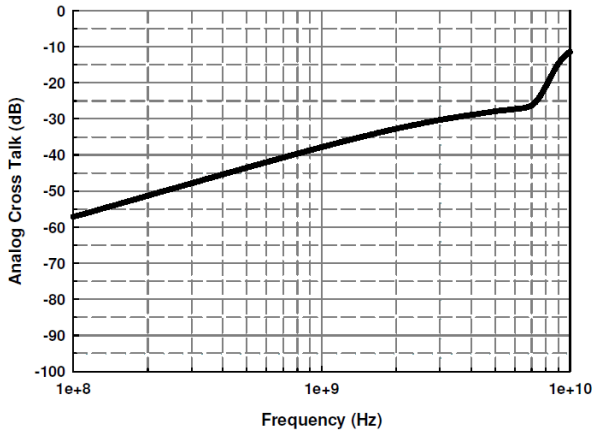
3. Transmission Line Pulsing (TLP) Measurement



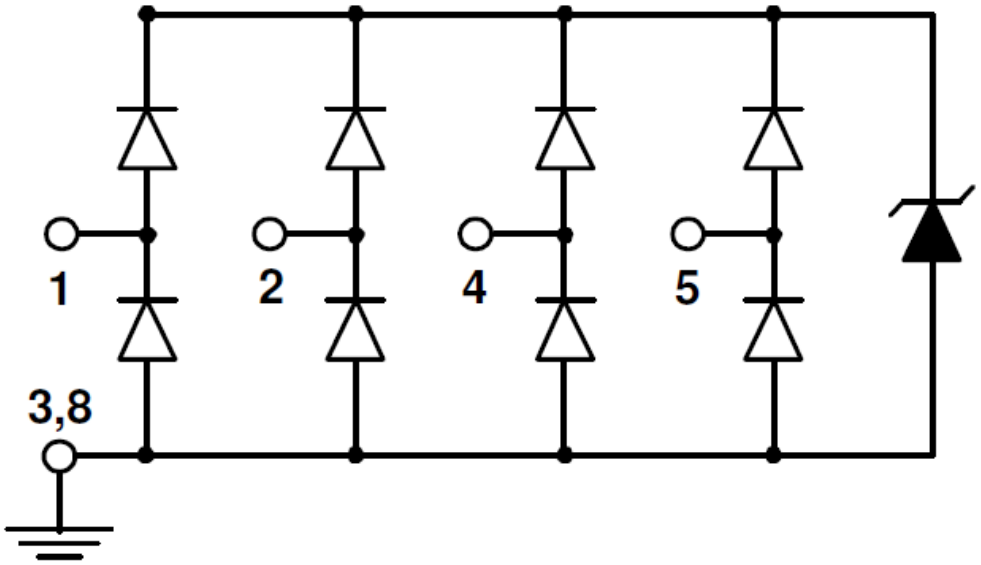
4. Insertion Loss S_{DD}



5. Analog Cross Talk



CIRCUIT DIAGRAM



APPLICATION INFORMATION

The 174S-04F is designed to protect four data lines from transient over-voltage (such as ESD stress pulse). The device connection of 174S-04F is shown in the Fig. 1. In Fig. 1, the four protected data lines are connected to the ESD protection pins (pin1, pin2, pin4, and pin5) of 174S-04F. The ground pins (pin3 and pin8) of 174S-04F are the negative reference pins.

These pins should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should be kept as short as possible.

174S-04F can provide ESD protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

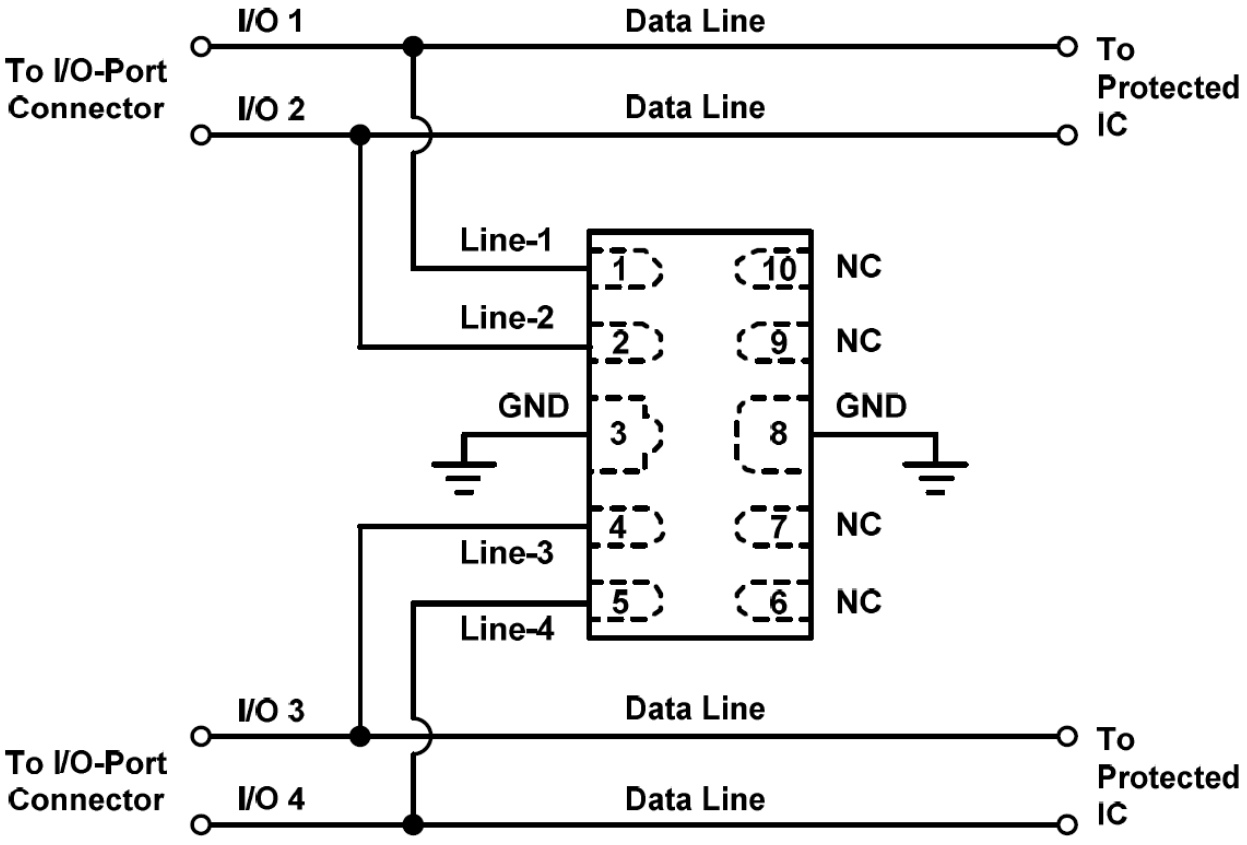
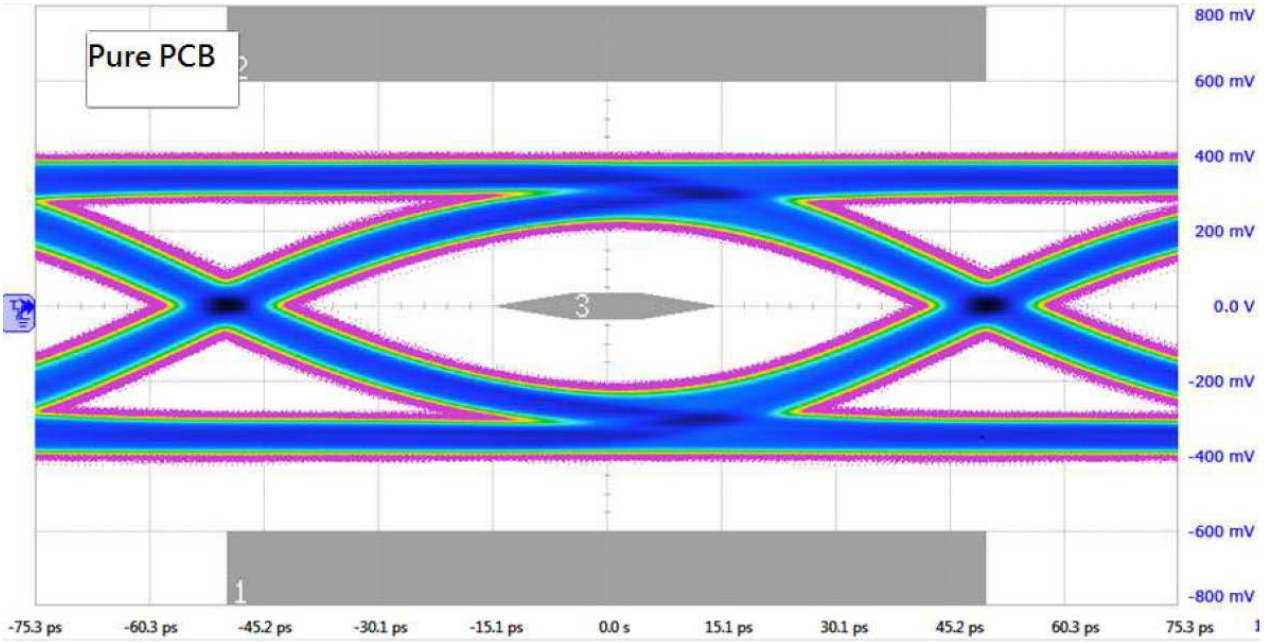


Fig. 1 Data lines connection of 174S-04F.

Fig. 2 shows the USB3.1 (10 Gb/s) eye diagrams with and without 174S-04F. Due to the ultra-low capacitance, 174S-04F can be used for USB3.1 application.

Without 174S-04F



With 174S-04F

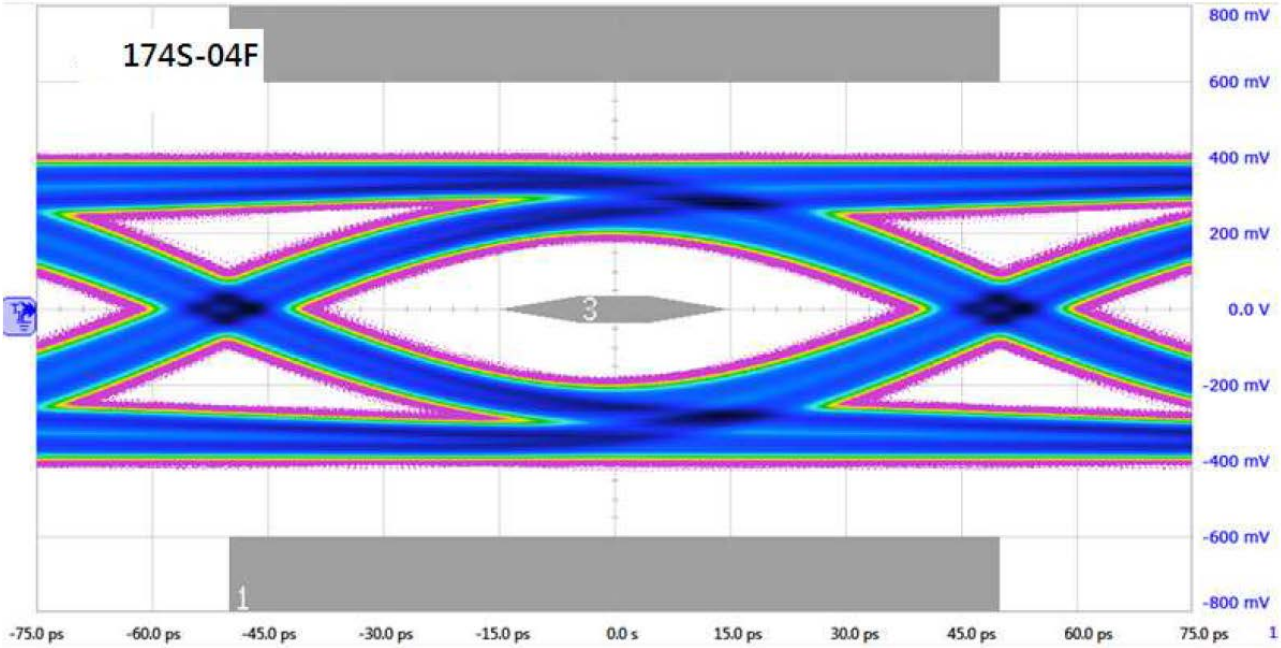
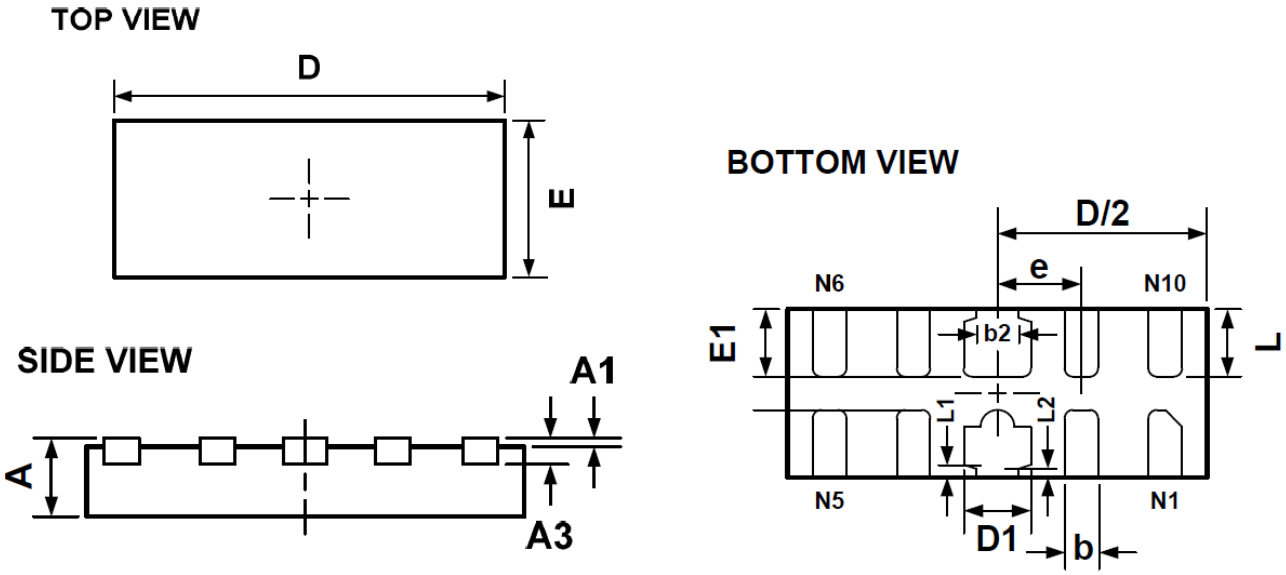


Fig. 2 USB3.1 (10Gb/s) eye diagrams with and without 174S-04F.

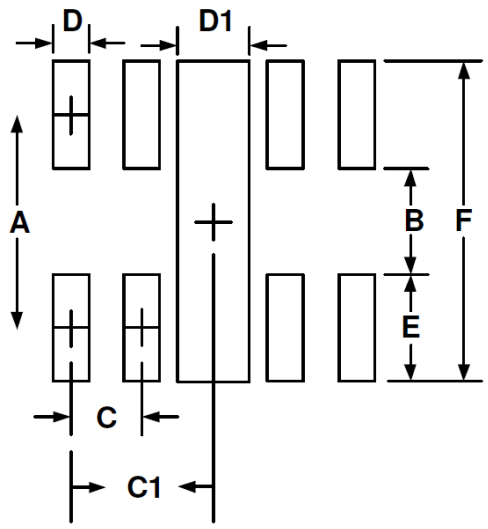
PACKAGE INFORMATION

Dimension in DFN10 (Unit: mm)



Symbol	Min	Max
A	0.400	0.550
A1	-	0.050
A3	0.152REF	
D	2.450	2.550
E	0.950	1.050
D1	0.350	0.450
E1	0.350	0.450
b	0.150	0.250
e	0.500 BSC	
L1	0.075 REF	
L2	0.050 REF	
b2	0.200	0.300
L	0.350	0.450

LAND LAYOUT



Index	Millimeter	Inches
A	0.875	0.034
B	0.20	0.008
C	0.50	0.02
C1	1.00	0.039
D	0.25	0.01
D1	0.4	0.016
E	0.675	0.027
F	1.55	0.061

Notes: This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

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