## DESCRIPTION

A7442A is a High Efficiency, Dual Outputs Synchronous DC-DC Buck Converters with CV/CC modes, which can output up to 21 W in a wide range input from 6 V to 36 V. A7442A operates either in Constant Output Voltage (CV) mode or Constant Output Current (CC) mode and provides a separated current limit function for each channel. In order to achieve better EMI performance and comply with Apple's MFi standard, the switching frequency was fixed at 130 kHz. A7442A is capable to operate in CC mode down to 3 V output voltage to protect the soft-short condition that is from the over current of the portable device
Other features including output Over Voltage Protection (OVP), Soft-start, hiccup mode output Under Voltage Protection (UVP), thermal shutdown (TSD), input UVLO. The hiccup mode output UVP can reduce the average input current to 50 mA.

The A7442A is available in PSOP8 package.

## ORDERING INFORMATION

<table>
<tr><th>Package Type</th><th colspan="2">Part Number</th></tr>
<tr><td rowspan="2">PSOP8<br>SPQ: 4,000pcs/Reel</td><td rowspan="2">MP8</td><td>A7442AMP8R</td></tr>
<tr><td>A7442AMP8VR</td></tr>
<tr><td>Note</td><td colspan="2">V: Halogen free Package<br>R: Tape & Reel</td></tr>
<tr><td colspan="3">AiT provides all RoHS products</td></tr>
</table>

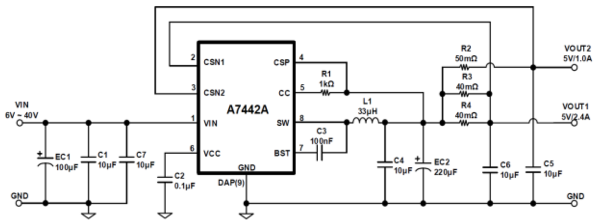
## FEATURES

- Wide Range Input Supply Voltage from 6V - 40V
- Up to 4.2 A Output Current
- up to 94 % Efficiency
- 130 kHz Fixed Switching Frequency, Easy EMI design
- Internal Soft-start Circuitry
- Built-in Input OVP, UVLO
- Compensation for Output Cord Voltage Drop
- Adjustable Constant Current Limits
- Output Over Voltage Protection
- Cycle by cycle Peak current Limit
- Hiccup Mode Output UVP for Soft-short < 3 V
- Thermal Shutdown
- Available in PSOP8 Package

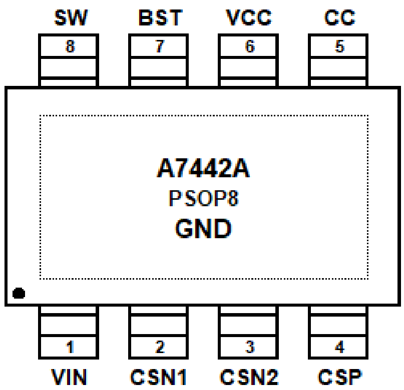
## APPLICATION

- Car Charger
- Portable Charging Devices
- CV/CC regulation DC/DC converter

## TYPICAL APPLICATION



## PIN DESCRIPTION




Top View

| Pin # | Symbol | Function |
|---|---|---|
| 1 | $V_{IN}$ | Input Voltage Supply. Connect a decoupling capacitor between $V_{IN}$ and GND pins with least distance. |
| 2 | CSN1 | Channel 1 Current Limit Negative Feedback pin. Kevin sensing from this pin to the sensing resistor is recommended. |
| 3 | CSN2 | Channel 2 Current Limit Negative Feedback pin. Kevin sensing from this pin to the sensing resistor is recommended. |
| 4 | CSP | Current Limit Common and Output Voltage Feedback pin. Kevin sensing from this pin to the center point of both sensing resistors is recommended. |
| 5 | CC | Cable Compensation pin. Connect a resistor to CSP to adjust cord compensation gain. |
| 6 | $V_{CC}$ | Internal 5V Power Supply. Connect a 100nF capacitor between $V_{CC}$ and GND pins for stability and noise de-coupling. |
| 7 | BST | Boot-Strap pin. Supply input for the gate drive circuit of high-side NFET. Connect a 100nF capacitor between BST and SW pins. |
| 8 | SW | Switch Node between high-side NFET and low-side NFET. Connect this pin to the switching node of inductor. |
| DAP(9) | GND | Ground and Thermal Pad on the bottom of IC. Ground pin of internal circuitry and Power Return Pin for Sync-NFET source connection. |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| $V_{IN}$ | -0.3V ~ 42V |
| SW | -0.3V ~ ($V_{IN}$ + 0.2V) ≤ 42V |
| BST to SW | -0.3V ~ 6V |
| CSP, CSN1, CSN2, CC | -0.3V ~ 6V |
| $V_{CC}$ | -0.3V ~ 6V |
| ESD Rating (Human Body Model) | ±4kV NOTE1 |
| Package Thermal Resistance NOTE2 | |
| $R_{θJA}$ | 50°C/W |
| $T_J$, Min. Operating | -40°C |
| $T_J$, Max. Operating | Internally Limited |
| Storage Temperature | -55°C ~ 150°C |
| Lead Temperature (Soldering 10 sec.) | 260°C |

Stress beyond above listed "Absolute Maximum Ratings" may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE1: Tested and classified as Class 3A per ESDA/JEDEC JDS-001-2014.

NOTE2: Thermal Resistance is measured in the natural convection at $T_A$ = 25 °C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

## ELECTRICAL CHARACTERISTICS[NOTE3]

$V_{IN}$ = 12V, $T_A$ = 25°C, unless otherwise noted.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Input Supply Voltage** | | | | | | |
| Input Voltage | $V_{IN}$ | | 6 | - | 40 | V |
| **Input UVLO & OVP** | | | | | | |
| UVLO Threshold | $V_{UVLO}$ | $V_{IN}$ Rising | 3.93 | 4.37 | 4.82 | V |
| OVP Threshold[NOTE4] | $V_{IN\_OVP}$ | $V_{IN}$ Rising | 36.5 | 39.5 | - | V |
| OVP Hysteresis[NOTE4] | $V_{IN\_OVPHYS}$ | $V_{IN}$ Falling | - | 2.5 | - | V |
| **Input Supply Current** | | | | | | |
| Quiescent Current (non-switching) | $I_Q$ | $V_{OUT}$ = 5.3V | 380 | 470 | 560 | μA |
| **Output Voltage** | | | | | | |
| Output Voltage Regulation | $V_{CSP}$ | No Load | 5.00 | 5.08 | 5.15 | V |
| CSP OVP Upper Threshold | $V_{OVP}$ | $V_{CSP}$ Rising | 5.65 | 6.00 | 6.18 | V |
| CSP OVP Hysteresis | $V_{CSP\_HYS}$ | $V_{CSP}$ Falling | - | 270 | - | mV |
| CSP UVP Threshold | $V_{UVP}$ | | 2.84 | 3.01 | 3.19 | V |
| Cable Compensation Voltage NOTE4 | $V_{CCOMP}$ | $R_{CC}$=1kΩ, $I_{LOAD\_CH1}$=2.4A, $I_{LOAD\_CH2}$=0A, $R_S$=20mΩ | - | 96 | - | mV |
| | | $R_{CC}$=1kΩ, $I_{LOAD\_CH1}$=0A, $I_{LOAD\_CH2}$=1A, $R_S$=50mΩ | - | 100 | - | mV |
| **Oscillator** | | | | | | |
| Switching Frequency | $f_{SW}$ | $I_{LOAD}$=1A | 107 | 130 | 160 | kHz |
| Maximum Duty Cycle | $D_{MAX}$ | | - | 99 | - | % |

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **MOSFET** | | | | | | |
| High Side MOSFET On Resistance | $R_{DS(ON)H}$ | | - | 55 | - | mΩ |
| Low Side MOSFET On Resistance | $R_{DS(ON)L}$ | | - | 55 | - | mΩ |
| High-Side MOSFET Leakage Current | $I_{LEAK\_H}$ | CC = 6.5V, $V_{IN}$ = 12V, $V_{SW}$ = 0V | - | - | 15 | µA |
| Low-Side MOSFET Leakage Current | $I_{LEAK\_L}$ | CC=6.5V, $V_{SW}$ = 12V, $V_{IN}$ =12V | - | - | 15 | µA |
| **Current Limit** | | | | | | |
| High Side MOSFET Peak Current Limit | $I_{LIM\_HS}$ | $V_{OUT}$=5V | - | 7.0 | - | A |
| Channel 1 Constant Current Limit Threshold | $I_{CS1}$ | $R_{CS1}$=20mΩ | 2.85 | 3.05 | 3.25 | A |
| Channel 2 Constant Current Limit Threshold | $I_{CS2}$ | $R_{CS2}$=50mΩ | 1.14 | 1.22 | 1.30 | A |
| **Regulator** | | | | | | |
| $V_{CC}$ Regulator | $V_{CC\_5}$ | $T_A$ = 25 °C, 0 < $I_{CC}$ <5 mA | 4.541 | 4.896 | 5.109 | V |
| $V_{CC}$ Output Current | $I_{CC\_10}$ | $V_{IN}$ = 12V, $V_{CC}$ = 4.3V, $T_A$ = 25°C | 10 | - | - | mA |
| **Soft-start** | | | | | | |
| Soft-start Time | $t_{SS}$ | | - | 1 | - | ms |
| UVP Hiccup Interval[NOTE4] | $t_{UVP}$ | | - | 250 | - | ms |
| **Thermal Shutdown** | | | | | | |
| Thermal Shutdown Threshold NOTE3 | $T_{SDN}$ | | - | 165 | - | °C |
| Thermal Shutdown Hysteresis[NOTE3] | $T_{SDNHYS}$ | | - | 40 | - | °C |

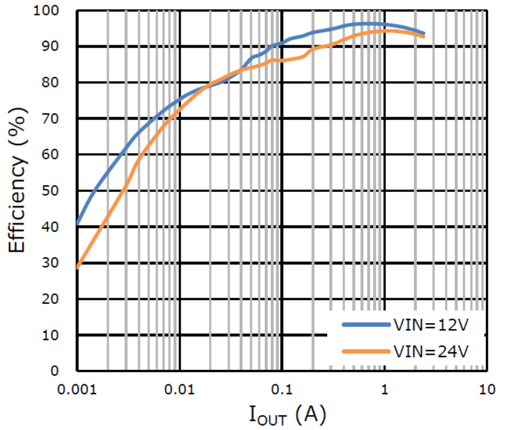
NOTE3: Specifications over temperature range are guaranteed by design and characterization.

NOTE4: Guaranteed by design and characterization only.

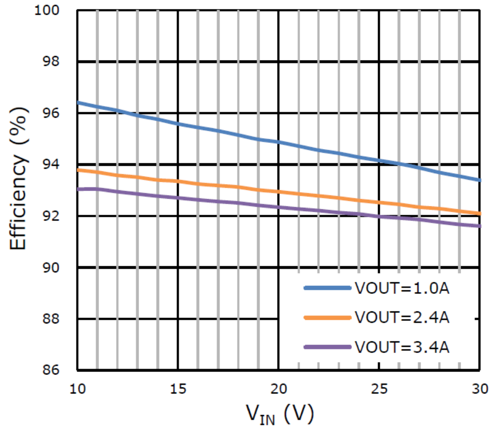
## TYPICAL PERFORMANCE CHARACTERISTICS

All curves taken at $V_{IN}$ = 12V with configuration in typical application circuit shown in this datasheet. $T_A$ = 25°C, unless otherwise specified.

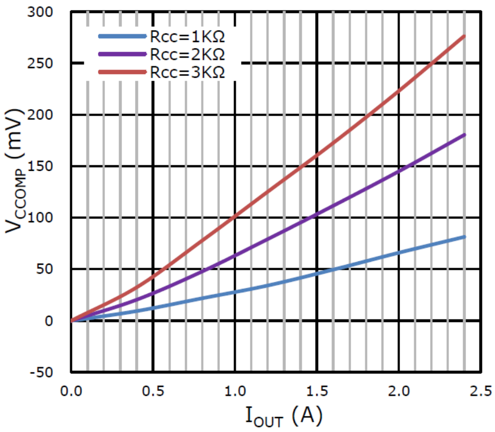
1. Output1 Efficiency vs. Load Current



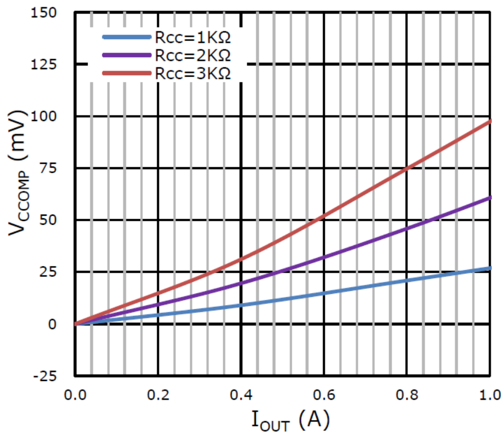

2. Output2 Efficiency vs. $V_{IN}$



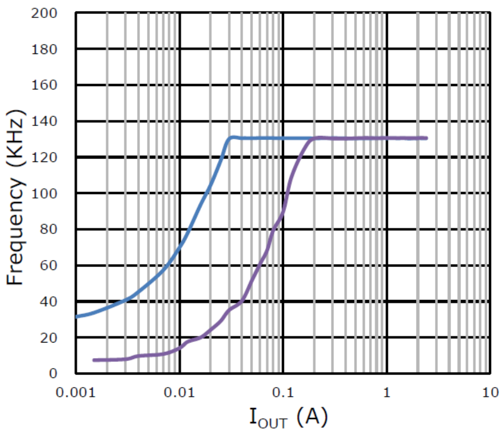

3. Cable Compensation $V_{CCOMP}$ vs. Output Current ($R_{CS}$=20mΩ)



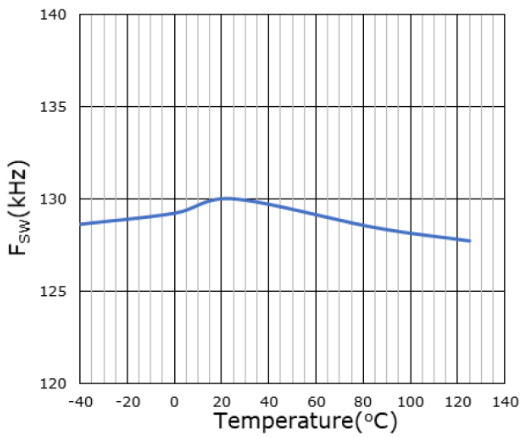

4. Cable Compensation $V_{CCOMP}$ vs. Output Current ($R_{CS}$=50mΩ)



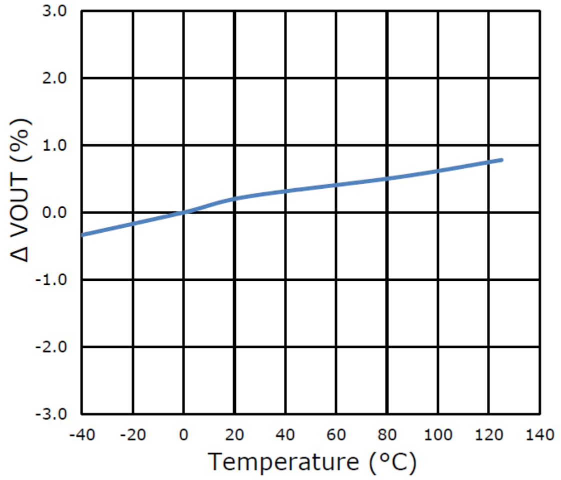

5. Switching Frequency vs. $I_{LOAD}$



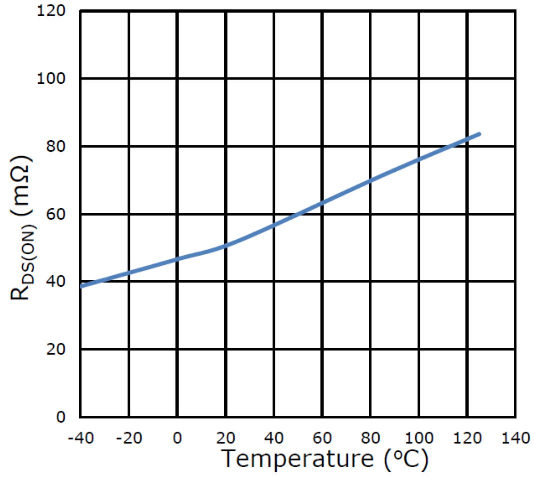

6. CCM Switching Frequency vs. Temperature



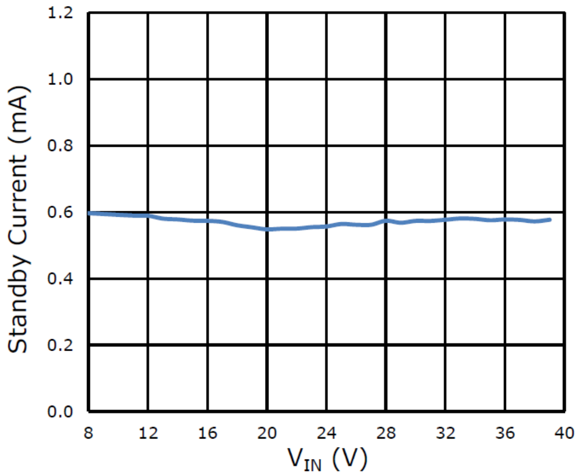
7. $V_{OUT}$ vs. Temperature



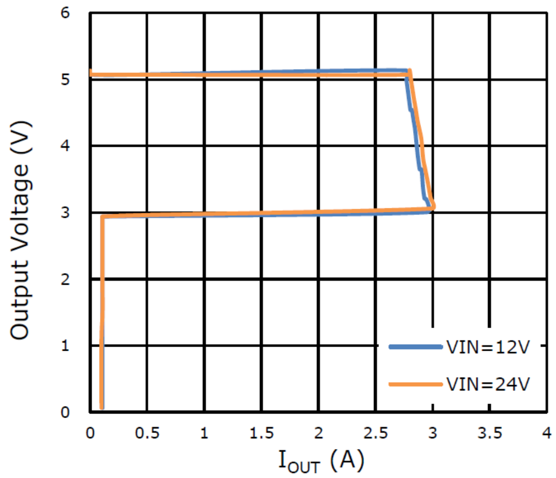

8. $R_{DS(ON)}$ vs. Temperature



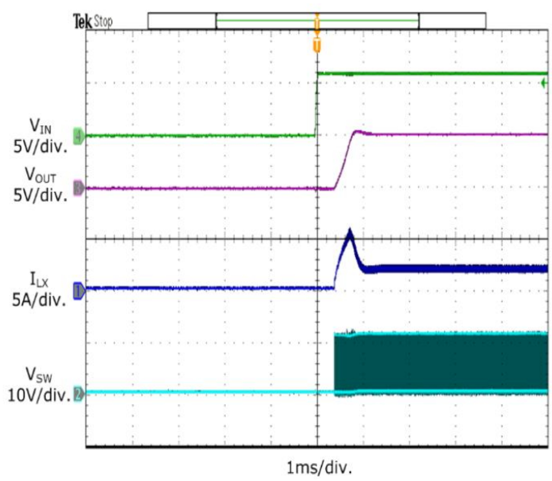

9. Quiescent Current vs. $V_{IN}$



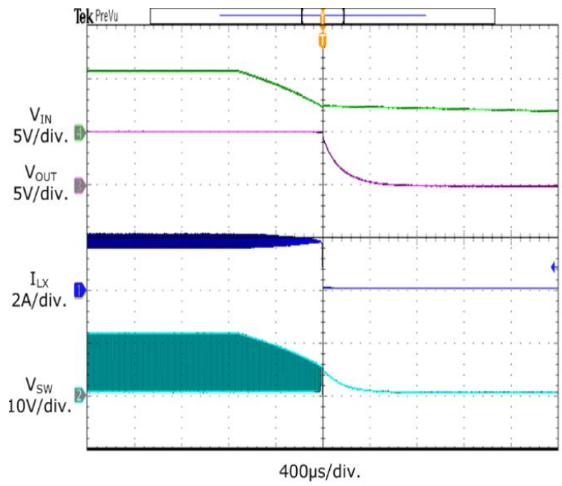

10. Output CC/CV Curve with $R_{CS}$ = 20mΩ



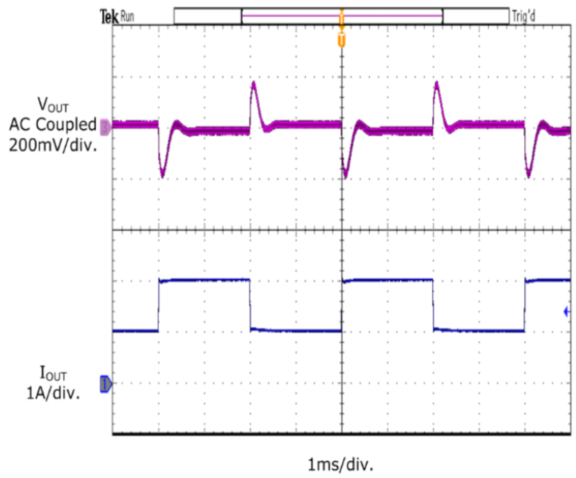

11. Power Up



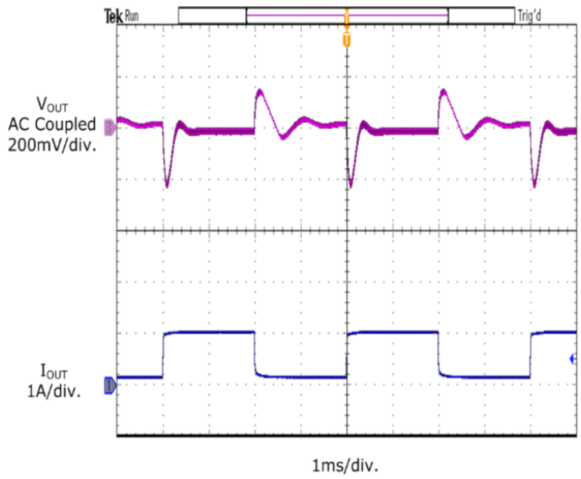

12. Power Down



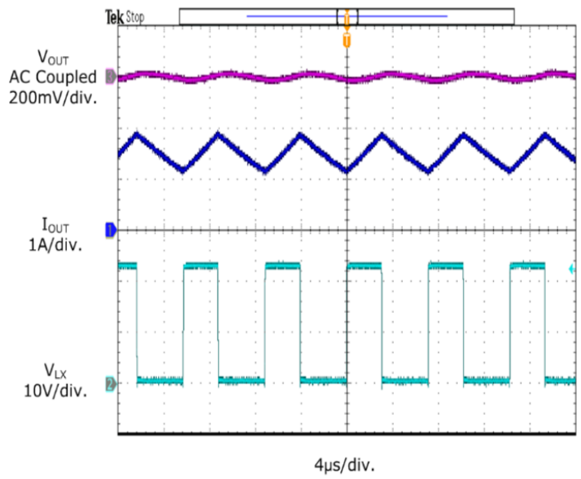
13. Load Transient



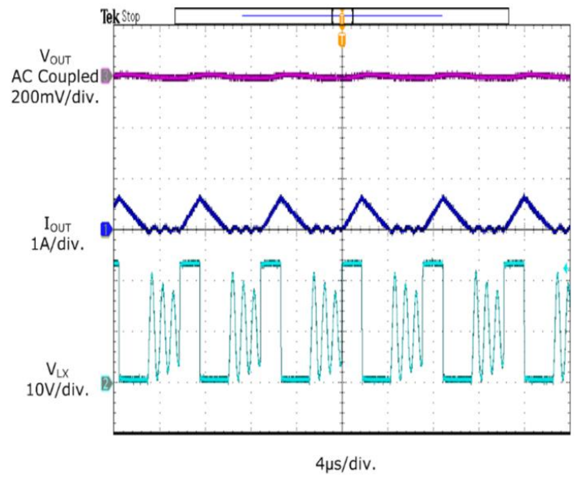

14. Load Transient



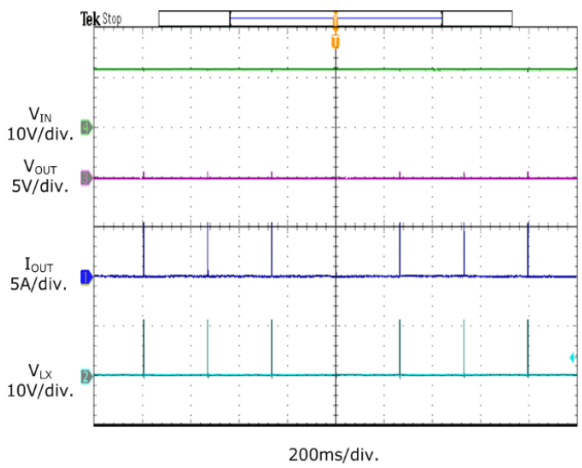

15. Continuous Mode Operation



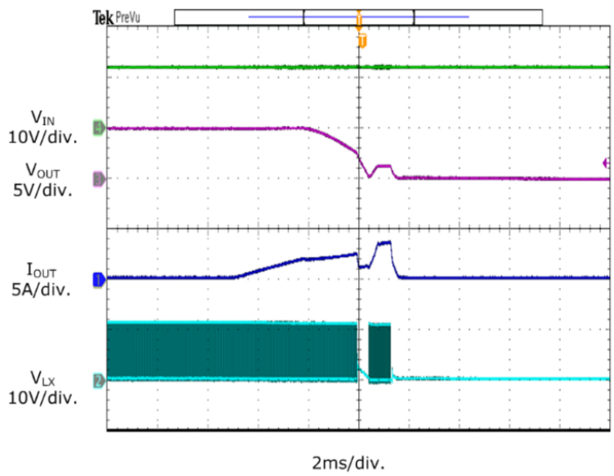

16. Discontinuous Mode Operation



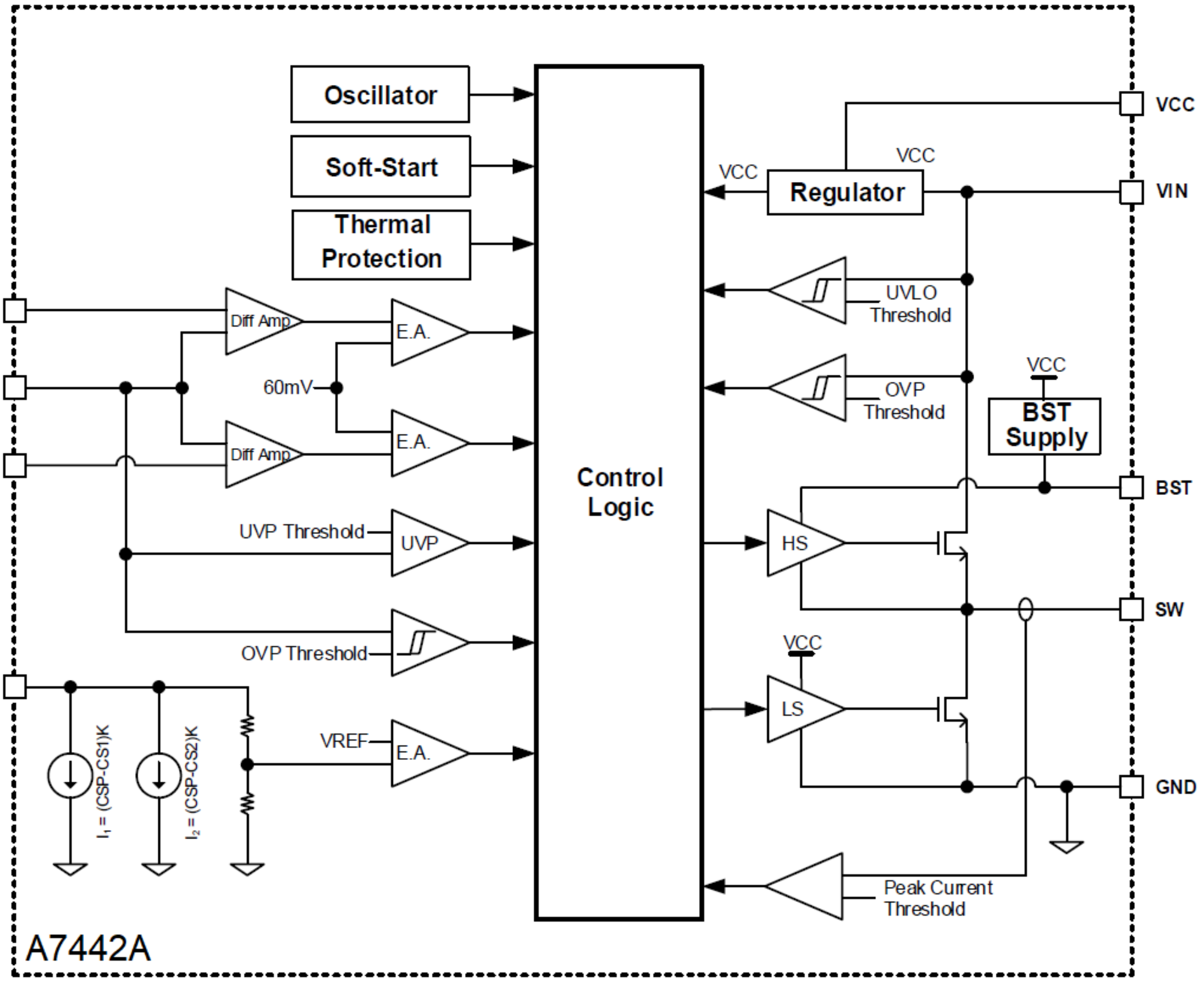

17. Short Circuit Protection




18. Short Circuit Protection (Zoom In)



## BLOCK DIAGRAM



## DETAILED INFORMATION

### Operation

The A7442A is a monolithic high efficiency synchronous CV / CC buck converter with dual outputs. It utilizes internal MOSFETs to achieve high efficiency and up to 4.2 A output current in a wide input range from 6 V to 36 V. The constant current limit thresholds for each output can be programed through the CSP, CSN1 and CSN2 pins individually. The A7442A is capable to operate in CC mode down to 3 V output voltage to protect the soft-short condition that is from the over current of the portable device.

With the slope compensated current mode PWM control, provides stable switching and cycle-by-cycle current limit for excellent load and line responses and protection of the internal switches. During normal operation, the internal main switch is turned on for a certain time to ramp up the inductor current at each rising edge of the internal oscillator, and turned off when the peak inductor current is above the error voltage. The current comparator limits the average inductor current. Once the main switch is turned off, the synchronous rectifier will be turned on immediately and stay on until either the inductor current decay to zero, as indicated by the zero current comparator or the beginning of the next clock cycle.

### Compensation for Output Cord Voltage Drop

In charger applications, the voltage drop across the output cord is significant in high current charging process. In some cases, excessive voltage drop across the output cord will even extend the charging time if high impedance output cord is used. The A7442A integrated a cable compensation function. When the output current increases, the CC pin sinks current into the IC to increase the voltage drop across the resistor, $R_{CC}$, in order to increase the output voltage. The sinking current of the CC pin is proportional to the voltage across CSP and CSN1 pins plus CSP and CSN2 pins. Thus, the cable compensation function can increase the output voltage according to the load. The increment of the voltage measured at CSP pin($V_{CSP}$) is called Cable Compensation Voltage ($V_{CCOMP}$). The value of $R_{CC}$ determines the gain of the cable compensation. The value of $R_{CC}$ can be calculated using Equation 1.

$$R_{CC} = \frac{V_{CCOMP}}{(I_{OUT1} \times R_{S1} + I_{OUT2} \times R_{S2}) \times K} \quad (1)$$

Where

- $R_{CC}$ is the value of the resistor between CC pin and the node of the inductor.
- $V_{CCOMP}$ is the cable compensation voltage measured at the CSP pin.
- $I_{OUT1}$ is the output current of channel 1.
- $I_{OUT2}$ is the output current of channel 2.
- K is a constant which is ~ 0.002A/V.
- $R_{S1}$ is the value of the sensing resistor of channel 1.
- $R_{S2}$ is the value of the sensing resistor of channel 2.

CV / CC Mode Control

The A7442A features a CV / CC function. It operates either in CV mode or CC mode. The CC limits for each channel can be programed through CSP, CSN1 and CSN2 pins individually.

The CC mode provides an accurate current limiting function which is programed through the sensing resistors, $R_{S1}$ and $R_{S2}$. Output current can increase until it reaches the CC limit set by the sensing resistors. At this point, the A7442A will transit from regulating output voltage to regulating output current, and the output voltage will drop with increasing load. The A7442A can output up to 4.2A current and provide dual output with individual CC limits. Figure 1. shows the CC limit verse sensing resistor, $R_{S1}$ or $R_{S2}$. The CC limit should be set at a level which is slightly higher than the required output current. For example, 2.4A and 1.0A outputs are required for channel 1 and channel 2 respectively. According to Figure 1. 20mΩ and 50mΩ sensing resistors should be selected for ensuring 2.4 A and 1.0 A continuous output currents is enough.

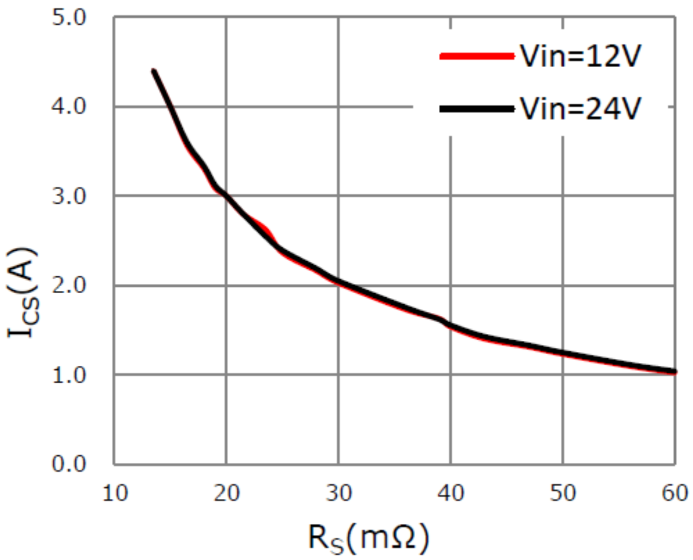



**Figure 1. CC Limit vs. $R_S$**

In CV mode, the voltage at CC pin is regulated at 5.1 V. The output voltage in no load condition is 5.1 V. The output voltages of channel 1($V_{OUT1}$) and the output voltages of channel 2($V_{OUT2}$) can be calculated using Equation 2.

$$V_{OUT*} = 5V + V_{CCOMP} - (I_{OUT*} \times R_{S*}) \qquad (2)$$

Where

- $V_{OUT*}$ is the output voltage of channel 1 or channel 2.
- $V_{CCOMP}$ is the cable compensation voltage measured at the CSP pin.
- $R_{CC}$ is the value of the resistor between CC pin and the node of the inductor.
- $I_{OUT*}$ is the output current of channel 1 or channel 2.
- $R_{S*}$ is the value of the sensing resistor of channel 1 or channel 2.

### Cycle by Cycle Peak Current Limit

The peak current limit prevents the A7442A from high inductor current and from drawing excessive current from the input voltage rail. Excessive current might occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the peak limit threshold, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current.

### Input Under-voltage Lockout (UVLO)

An input UVLO circuit prevents the converter from starting the operation until the input voltage rises above the typical UVLO threshold of 4.37 V.

### CSP Over Voltage Protection (OVP)

The CSP pin senses the output voltage at node between the sensing resistors, $R_{S1}$ and $R_{S2}$. If the voltage at CSP pin is detected above CSP OVP threshold of 5.8 V typically, the device stops switching immediately until the voltage at the CSP pin drops the hysteresis voltage lower than CSP OVP threshold. This function prevents the device as well as the output capacitors from damage by high voltage on the output even though the feedback loop is faulty broken, i.e. $R_{CC}$ is open.

### Input Over Voltage Protection (OVP)

The input OVP is an additional function to protect the device from damage in a condition which is above the specified input voltage range. Once the input voltage is raising above input OVP threshold, 39.5V typically, the A7442A stops switching to reduce the chance of damage by the voltage spike at SW pin. The device goes back to normal operation until the input voltage falls a hysteresis about 2.5V below the input OVP threshold.

### Hiccup Mode Output Under Voltage Protection (UVP)

There is a CSP UVP threshold. If the threshold is hit, the hiccup mode output UVP will be triggered by disabling the converter and restarts soft-start after a predefined interval about 0.25sec. The A7442A repeats this mode until the under voltage condition is removed. This function prevents the damage of the system from hard-short condition and the soft-short condition from the over current of portable device.

### Soft-start

The A7442A implements the soft start function to reduce the inrush current during startup. The soft start begins once the input voltage raises above UVLO threshold. The soft start time is typically 1ms.

### Thermal Shutdown

A thermal shutdown is implemented to prevent the damage due to excessive heat and power dissipation. Typically, the thermal shutdown happens at the junction temperature of 165°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature drops the hysteresis temperature lower than thermal shutdown threshold, then the device starts switching again.

## APPLICATIONS INFORMATION

### Design Requirement

| Design Parameters | Target Values |
|---|---|
| Input Voltage Range | 6V to 40V |
| Typical Input Voltage | 24V |
| Output Voltage | 5V |
| Channel 1 Output Current Rating | 2.4A |
| Channel 2 Output Current Rating | 1.0A |
| $V_{CCOMP}$ at Full Load | 200mV |

Table 1. Design Parameters

### Setting the CC Limit

The typical application circuit is showed on the front page. Table 2 shows the CC limit verse sensing resistor. According to this figure, $R_{S1}$ and $R_{S2}$ should be set at 20mΩ to output 2.4A continuous current and 50mΩ to output 1.0A continuous current respectively.

### Setting the Cable Compensation Resistor ($R_{CC}$)

The resistor, $R_{CC}$, solely determines the gain of the cable compensation. By subtitling $V_{CCOMP}$, $I_{OUT}$, $R_S$ and K into the Equation 1, $R_{CC}$ = 1kΩ. Table 2 and shows the cable compensation voltage at different load with $R_{CC}$ = 1kΩ, $R_{S1}$ = 20mΩ and $R_{S2}$ = 50mΩ.

| Total $I_{LOAD}$ (%) | Total $I_{LOAD}$ (A) | $I_{LOAD1}$ (A) | $I_{LOAD2}$ (A) | $V_{CCOMP}$ (mV) |
|---|---|---|---|---|
| 0 | 0.00 | 0.00 | 0 | 0 |
| 10 | 0.25 | 0.24 | 0.1 | 20 |
| 20 | 0.50 | 0.48 | 0.2 | 40 |
| 30 | 0.75 | 0.72 | 0.3 | 60 |
| 40 | 1.00 | 0.96 | 0.4 | 80 |
| 50 | 1.25 | 1.20 | 0.5 | 100 |
| 60 | 1.50 | 1.44 | 0.6 | 120 |
| 70 | 1.75 | 1.68 | 0.7 | 140 |
| 80 | 2.00 | 1.92 | 0.8 | 160 |
| 90 | 2.25 | 2.16 | 0.9 | 180 |
| 100 | 3.40 | 2.40 | 1 | 200 |

Table 2. Cable Compensation Voltage at Different Load

**Inductor Selection**

Since the selection of the inductor affects the power supply's steady state operation, transient behavior, loop stability, and overall efficiency, the inductor is the most important component in switch power regulator design. Three most important specifications to the performance of the inductor are the inductor value, DC resistance, and saturation current.

The A7442A designed to work with inductor values between 15μH to 47μH. A 15μH inductor is typically available in a smaller or lower-profile package, while a 47μH inductor produces lower inductor current ripple. If the output current is limited by the peak current limit of the IC, using a 47μH inductor can maximize the converter's output current capability.

The tolerance of inductors can be ranging from 10% to 30%. The inductance will further decrease 20% to 35% from the value of zero bias current depending on the definition of saturation by inductor manufacturers. The basic requirements of selecting an inductor are the saturation current must be higher than the peak switching current and the DC rated current is higher than the average inductor current in normal operation. In buck converter, the average inductor current is equal to the total output current. The inductor value can be derived from the Equation 3.

$$L=\frac{(V_{OUT}+V_{CCOMP})\times(V_{IN}-V_{OUT}-V_{CCOMP})}{V_{IN}\times\Delta I_L\times f_{SW}} \qquad (3)$$

Where

- $\Delta I_L$ is the inductor peak-to-peak ripple current.
- $V_{OUT}$ = 5 V (output voltage at no load).
- $V_{CCOMP}$ is the cable compensation voltage measured at the CSP pin.
- $V_{IN}$ is the input voltage.
- $f_{SW}$ is the switching frequency.

Lower inductor value results in higher ripple current and vice versa. Choose inductor ripple current approximately 30% of the maximum load current, 3.4A, or $\Delta I_L$ = 1.02A. By subtitling $V_{IN}$(typ.), $V_{OUT}$, $V_{CCOMP}$, $\Delta I_L$ and $f_{SW}$(typ.) into the above equation, the inductor value, L, is 30.7μH. The common inductor value is 33μH.

The saturation current of the inductor must be higher than the maximum output current, 3.4A, plus half of the inductor ripple current in worst case, i.e. highest operating $V_{IN}$(36V), lowest $f_{SW}$(107kHz), lowest inductor value(-10 ~ -30% from nominal value), to prevent the core from saturation. Table 3 lists a typical toroid inductor that meet target applications for the design requirements.

| Core Manufacturer | Core Part Number | L(μH) | No. of Turns | Wire Ø (mm) | μ | AL (nH/N²) | Size[ODxIDxH] (mm) |
|---|---|---|---|---|---|---|---|
| KDM Magnetic Powder Cores | KS040-125A | 33 ±10% | 23 | 0.7 | 125 | 66 | 10.20x5.08x3.96 |

Table 3. Recommended Toroid Inductor

### Input Capacitor Selection

The input capacitor reduces the surge current drawn from the input and switching noise from the device. The input capacitor impedance at the switching frequency should be less than the input source impedance to prevent high frequency switching current passing to the input. A low ESR input capacitor sized for maximum RMS current must be used. Multilayer Ceramic Capacitor (MLCC) with X5R or X7R dielectric is highly recommended because of their low ESR, low temperature coefficients and compact size characteristics. A 22μF MLCC is sufficient for most of applications.

### Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and to ensure regulation loop stability. The output capacitor must have low impedance at the switching frequency. MLCC with X5R or X7R dielectric is recommended due to their low ESR and compact size characteristics. The output ripple, $\Delta V_{OUT}$, is determined by:

$$\Delta V_{OUT} \le \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L} \times \left( ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right) \qquad (4)$$

### Layout Considerations

When doing the PCB layout, the following suggestions should be taken into consideration to ensure proper operation of the A7442A. These suggestions are also illustrated graphically in Figure 2 and Figure 3.

1. The power path including the GND trace, the SW trace and the $V_{IN}$ trace should be as short as possible, direct and wide.
2. The cable compensation resistor must be connected to the center point of both sensing resistors directly.
3. The input decoupling MLCC should be placed as close to the $V_{IN}$ and GND pins as possible and connected to input power plane and ground plane directly. This capacitor provides the AC current to the internal power MOSFET.
4. The power path between the output MLCC, $C_4$, and the power inductor should be keep short and the other terminal of the capacitor should connect to the ground plane directly to reduce noise emission.
5. Keep the switching node, SW, away from the sensitive cable compensation path.
6. Keep the negative terminals of input capacitor and output capacitor as close as possible.

7. Use Kelvin sense connection technique from the sensing resistors, $R_{S1}$ and $R_{S2}$, pads directly to the CSP, CSN1 and CSN2 pins to achieve accurate CC limit.
8. Use large copper plane and thermal vias for GND for best heat dissipation and noise immunity.

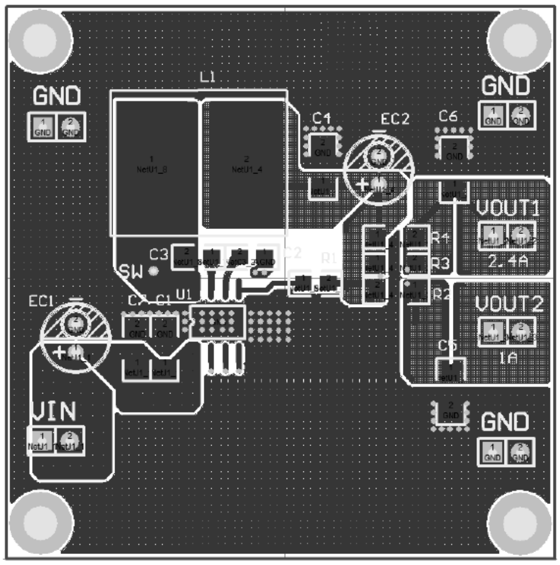



Figure 2. Top Layer

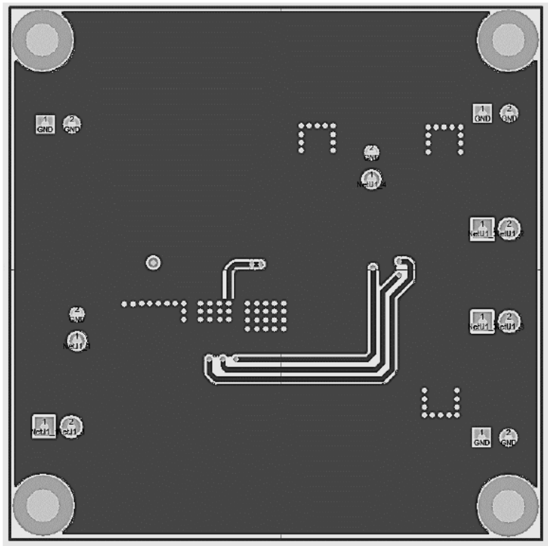
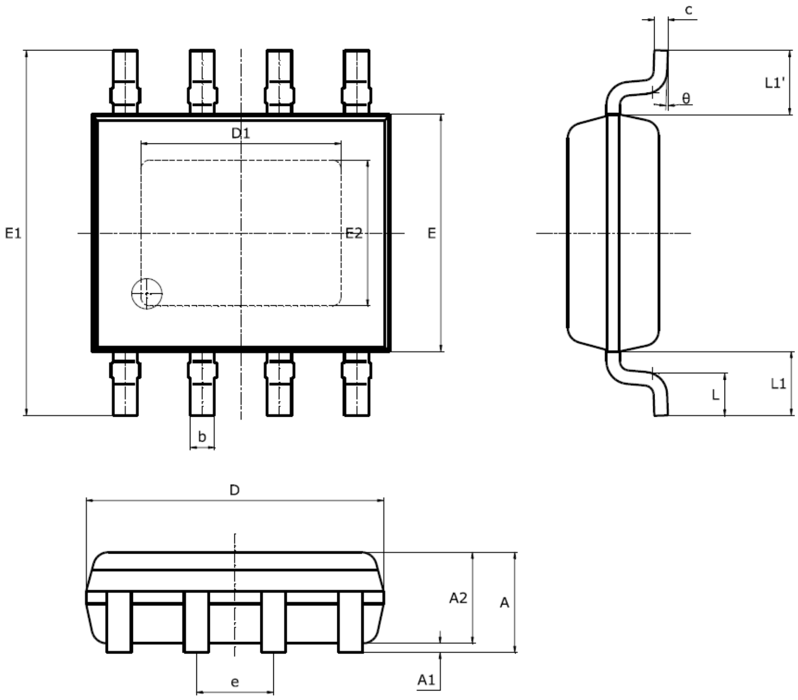


Figure 3. Bottom Layer

## PACKAGE INFORMATION

Dimension in PSOP8 (Unit: mm)




| Symbol | Millimeters | | Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.400 | 1.700 | 0.055 | 0.067 |
| A1 | 0.050 | 0.150 | 0.002 | 0.006 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.007 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| D1 | 3.202 | 3.402 | 0.126 | 0.134 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| E2 | 2.313 | 2.513 | 0.091 | 0.099 |
| e | 1.270 BSC | | 0.050 BSC | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| L1 | 1.040 REF | | 0.041 REF | |
| L1-L1’ | - | 0.120 | - | 0.005 |
| θ | 0° | 8° | 0° | 8° |

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