DESCRIPTION

AL595 contain an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Separate clocks are provided for both the shift register and storage register.

The shift register has an asynchronous reset ($\overline{MR}$) input, serial (SER) input, and serial outputs (Q7S) for cascading. A low on $\overline{MR}$ will clear the shift register. Data is shifted on the LOW-to-HIGH transitions of the SRCLK input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the RCLK input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ($\overline{OE}$) is Low. A High on $\overline{OE}$ causes the outputs to assume a high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the registers.

The AL595 is available in SOP16, TSSOP16, and QFN16 packages.

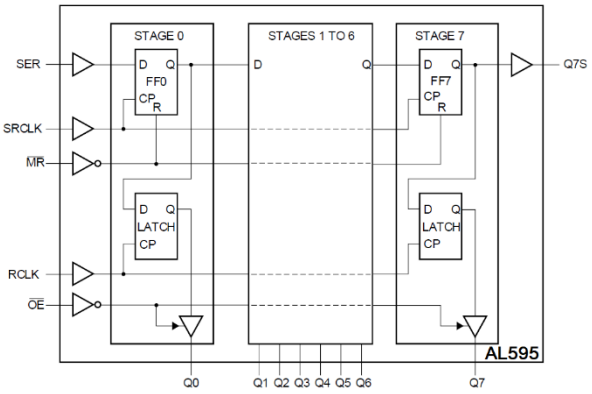
FEATURES

- 8-bit serial input, parallel output shift
- Wide operating voltage of 2V to5.5V
- Serial Output (Q7S)
- Low power consumption: 160μA(Max)
- Low input current:1μA(Max)
- Shift register has direct clear
- Storage register with 3-state outputs
- Extended Temperature: -40°C to +125°C

APPLICATION

- Network switches
- Power infrastructure
- LED displays
- Enterprise and communications
- Industrial
- Personal electronics
- Servers

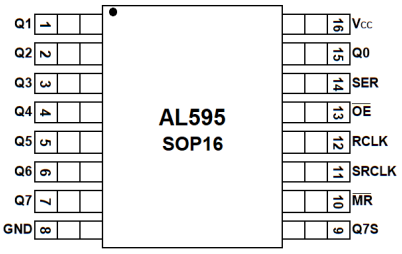
TYPICAL APPLICATION



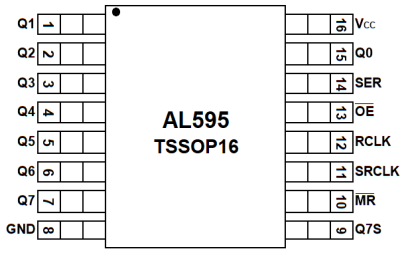
ORDERING INFORMATION

Package Type	Part Number	
SOP16 SPQ: 4,000pcs/Reel	M16	AL595M16R
		AL595M16VR
TSSOP16 SPQ: 4,000pcs/Reel	TMX16	AL595TMX16R
		AL595TMX16VR
QFN16 SPQ: 5,000pcs/Reel	Q16	AL595Q16R
		AL595Q16VR
Note	V: Halogen Free Package R: Tape & Reel	
AiT provides all RoHS products		

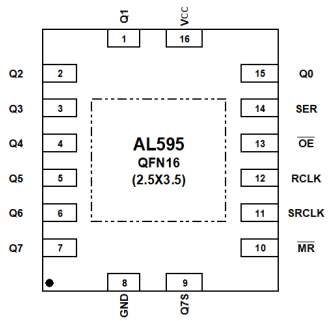
PIN DESCIPTION



SOP16, M16
Top View



TSSOP16, TMX16
Top View



QFN16, Q16
Top View

Pin #			Symbol	Type	Description
SOP16	TSSOP16	QFN16			
1~7			Q1~Q7	O	Parallel data output
8			GND	G	Ground
9			Q7S	O	Serial data output
10			$\overline{MR}$	I	Master reset (active Low)
11			SRCLK	I	Shift register clock input
12			PCLK	I	Storage register clock input
13			$\overline{OE}$	I	Output enable input (active Low)
14			SER	I	Serial data input
15			Q0	I	Parallel data output
16			V_{CC}	P	Supply voltage

FUNCTION TABLE

Control				Input	Output		Function
SRCLK	RCLK	$\overline{OE}$	$\overline{MR}$	SER	Q7S	Qn	
X	X	L	L	X	L	NC	a Low-level on $\overline{MR}$ only affects the shift registers
X	↑	L	L	X	L	L	empty shift register loaded into storage register
X	X	H	L	X	L	Z	shift register clear; parallel outputs in high-impedance Off-stage
↑	X	L	H	H	Q6S	NC	logic High-level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	L	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	L	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

H = HIGH Voltage State L = LOW Voltage State ↑ = LOW-to-HIGH Transition X = Don't Care
NC = No Change Z =High-Impedance OFF-State

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

V_{CC}, Supply Voltage Range		+6.5V
I_{IK}, Input Clamp Current	V_I<-0.5V or V_I>V_{CC}+0.5V	±20mA
I_{OK}, Output Clamp Current	V_O<-0.5V or V_O>V_{CC}+0.5V	±20mA
I_O, Output Current	V_O=-0.5V to (V_{CC}+0.5V)	
	Pin Q7S	±25mA
	Pin Qn	±35mA
I_{CC}, Supply Current		+70mA
I_{GND}, Ground Current		-70mA
θ_{JA}, Package thermal impedance (2)	SOP16	150°C/W
	TSSOP16	45°C/W
T_J, Junction Temperature (3)		-40°C ~ +150°C
T_{STG}, Storage Temperature		-65°C ~ +150°C
ESD Ratings		
$V_{(ESD)}$, Electrostatic Discharge	Human-Body Model (HBM), per ANSI/ESDA/JEDEC JS-001(4)	±4000V
	Charged-Device Model (CDM), per ANSI/ESDA/JEDEC JS-002(5)	±1500V
	Machine Model (MM)	±400V

Stress beyond above listed "Absolute Maximum Ratings" may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The package thermal impedance is calculated in accordance with JESD-51.

(3) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and TA. The maximum allowable power dissipation at any ambient temperature is P_D = ($T_{J(MAX)}$ - T_A) / $R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

(4) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(5) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

RECOMMENDED OPERATING CONDITIONS

Voltages are reference to GND(0V).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}		2.00	-	5.50	V
High-Level Input Voltage	V_{IH}	V_{CC}=2.0V	1.50	-	-	V
		V_{CC}=4.5V	3.15	-	-	
		V_{CC}=5.5V	3.85	-	-	
Low-Level Input Voltage	V_{IL}	V_{CC}=2.0V	-	-	0.50	V
		V_{CC}=4.5V	-	-	1.35	
		V_{CC}=5.5V	-	-	1.65	
Input Voltage	V_I		0	-	V_{CC}	V
Output Voltage	V_O		0	-	V_{CC}	V
Input Transition Rise Or Fall Rate(Δt/Δv)	Data inputs	V_{CC}=2.0V	-	-	625	Ns/V
		V_{CC}=4.5V	-	-	139	
		V_{CC}=5.5V	-	-	83	
Operating temperature	T_A		-40	-	125	℃

OPERATING CHARACTERISTICS

T_A=25°C

Parameter	Conditions	Typ.	Unit
C_{pd}[1]	f_i = 1 MHz; V_I = GND to V_{CC} [2][3]	115	pF

(1) Power dissipation capacitance per transceiver.

(2) C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:

f_i = input frequency in MHz;

f_O = output frequency in MHz;

$\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

(3) All 9 outputs switching.

ELECTRICAL CHARACTERISTICS

Parameter		Conditions	Temp	Min. (1)	Typ. (2)	Max. (1)	Unit
V_{OH}		all outputs					V
		I_O=-20μA, V_{CC}=2.0V	FULL	1.9	-	-	
		I_O=-20μA, V_{CC}=4.5V		4.4	-	-	
		I_O=-20μA, V_{CC}=5.5V		5.4	-	-	
		Q7S output					
		I_O=-4mA, V_{CC}=4.5V	FULL	3.7	-	-	
		I_O=-5.2mA, V_{CC}=5.5V		4.7	-	-	
		Qn bus driver outputs					
		I_O=-6mA, V_{CC}=4.5V	FULL	3.7	-	-	
		I_O=-7.8mA, V_{CC}=5.5V		4.7	-	-	
V_{OL}		all outputs					V
		I_O=20μA, V_{CC}=2.0V	FULL	-	-	0.1	
		I_O=20μA, V_{CC}=4.5V		-	-	0.1	
		I_O=20μA, V_{CC}=5.5V		-	-	0.1	
		Q7S output					
		I_O=4mA, V_{CC}=4.5V	FULL	-	-	0.4	
		I_O=5.2mA, V_{CC}=5.5V		-	-	0.4	
		Qn bus driver outputs					
		I_O=6mA, V_{CC}=4.5V	FULL	-	-	0.4	
		I_O=-7.8mA, V_{CC}=5.5V		-	-	0.4	
I_I	Input Leakage Current	V_I=V_{CC} or GND, V_{CC}=5.5V	FULL	-	-	±1	μA
I_{OZ}	OFF-State Output Current	V_I =V_{IH} or V_{IL}, V_O=V_{CC} or GND, V_{CC}=5.5V	FULL	-	-	±10	
I_{CC}	Supply Current	V_I=V_{CC} or GND, I_O=0A, V_{CC}=5.5V	FULL	-	-	160	
C_I	Input Capacitance	V_I=V_{CC} or GND, V_{CC}=3.3V	FULL	-	3.5	500	

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

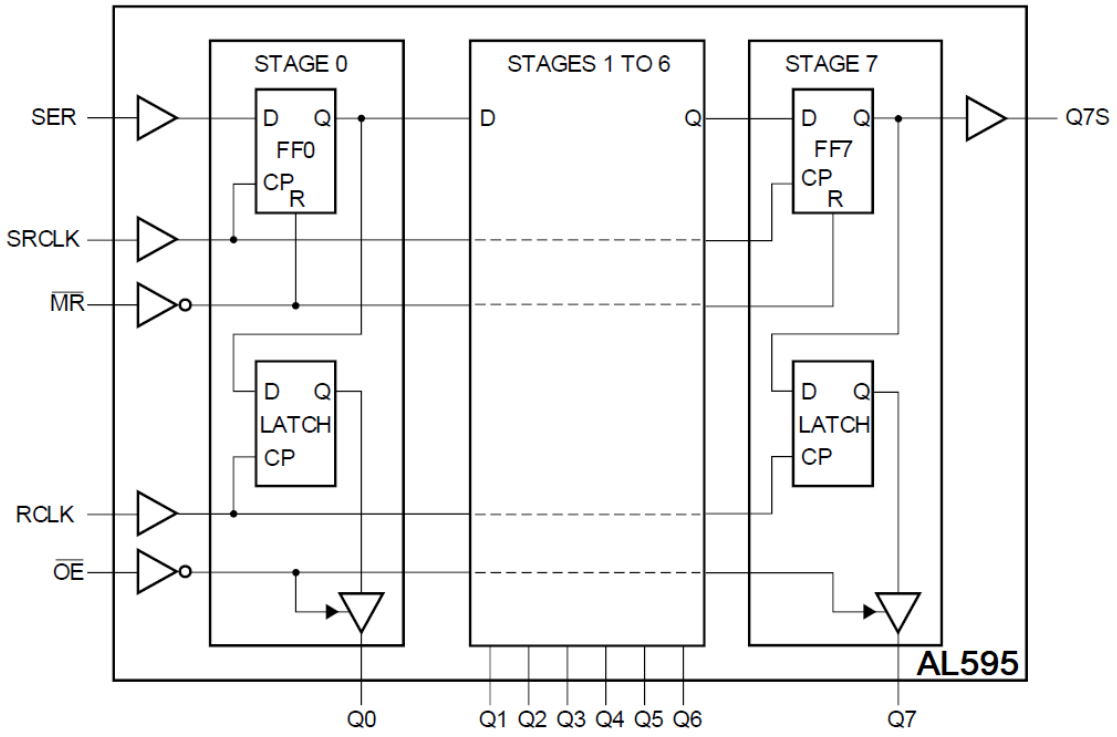
SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (-40°C to 125°C, unless otherwise noted.) (1)

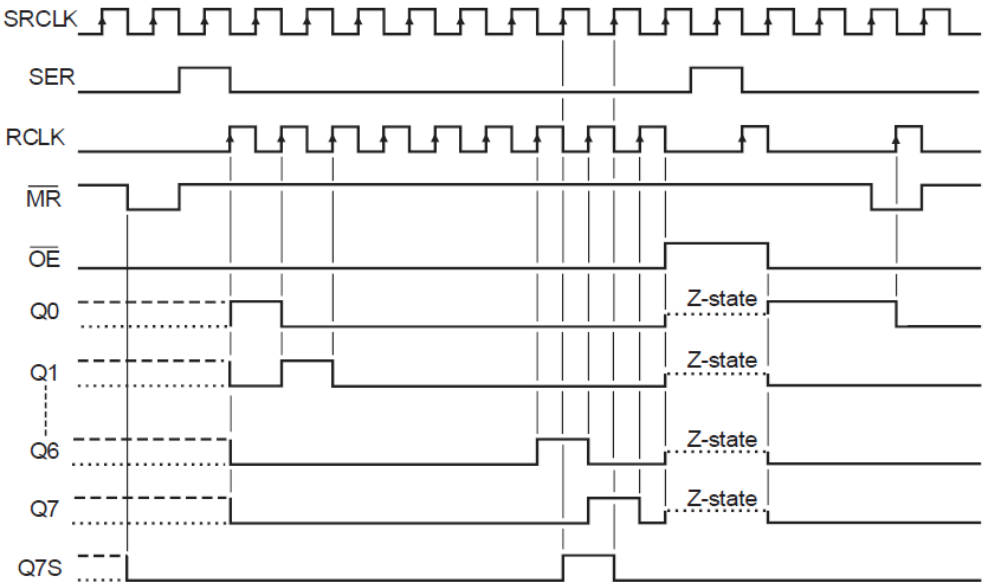
Parameter	V_{CC}=2.0V (2)			V_{CC}=4.5V (2)			V_{CC}=5.5V (2)			Unit
	Min.	Typ. (3)	Max.	Min.	Typ. (3)	Max.	Min.	Typ. (3)	Max.	
Propagation Delay,t_{pd}(4) SRCLK to Q7S	-	-	42	-	-	18	-	-	16	ns
Propagation Delay, t_{pd} RCLK to Qn	-	-	40	-	-	18	-	-	18	ns
High to Low Propagation, $\overline{MR}$ to Q7S, t_{PHL}(5)	-	-	28	-	-	14	-	-	10	ns
Enable Time,t_{en}(6) $\overline{OE}$ to Qn	-	-	36	-	-	16	-	-	12	ns
Disable Time,t_{dis}(7) $\overline{OE}$ to Qn	-	-	50	-	-	41	-	-	38	ns
Pulse Width, t_w SRCLK High or Low	110	-	-	22	-	-	19	-	-	ns
Pulse Width, t_w RCLK High or Low	110	-	-	22	-	-	19	-	-	ns
Pulse Width, t_w $\overline{MR}$ Low	110	-	-	22	-	-	19	-	-	ns
Hold Width,t_h SER to SRCLK	3	-	-	3	-	-	3	-	-	ns
Set-Up Time,t_{su} SER to SRCLK	75	-	-	15	-	-	13	-	-	ns
Set-Up Tme,t_{su} SRCLK to RCLK	110	-	-	22	-	-	19	-	-	ns
Recovery Time t_{rec} $\overline{MR}$ to SRCLK	75	-	-	15	-	-	13	-	-	ns
Maximum Frequency f_{max} SRCLK/RCLK CL=15pF	4	-	-	20	-	-	24	-	-	MHz

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
(2) This parameter is ensured by design and/or characterization and is not tested in production.
(3) Typical values are measured at nominal supply voltage.
(4) t_{pd} is the same as t_{PHL} and t_{PLH}.
(5) t_{pd} is the same as t_{PHL} only.
(6) t_{en} is the same as t_{PZL} and t_{PZH}.
(7) t_{dis} is the same as t_{PLZ} and t_{PHZ}

BLOCK DIAGRAM

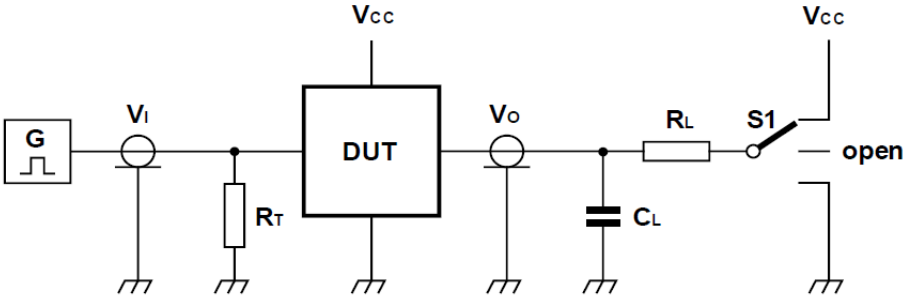


TIMING DIAGRAM



DETAILED INFORMATION

Parameter Measurement Information



LOAD CIRCUIT

TEST	S1
t_{PHL}/t_{PLH}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
V_I	V_{CC}
t_r/t_F	6ns
C_L	50pF
R_L	1KΩ

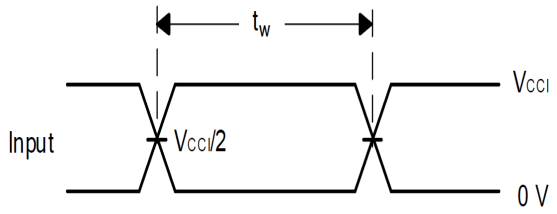


Figure 1. Voltage Waveforms Pulse Duration

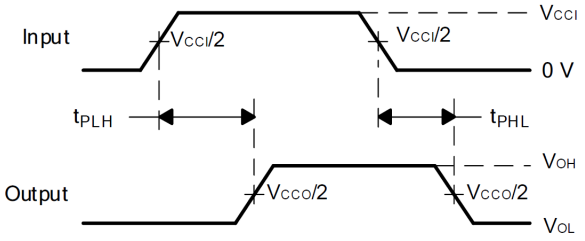


Figure 2. Voltage Waveforms Propagation Delay Times

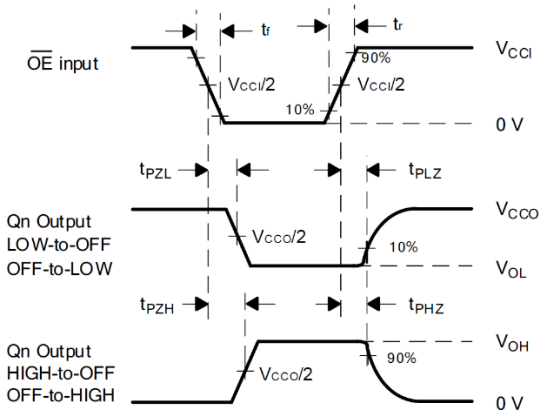


Figure 3. Voltage Waveforms Enable and Disable Times

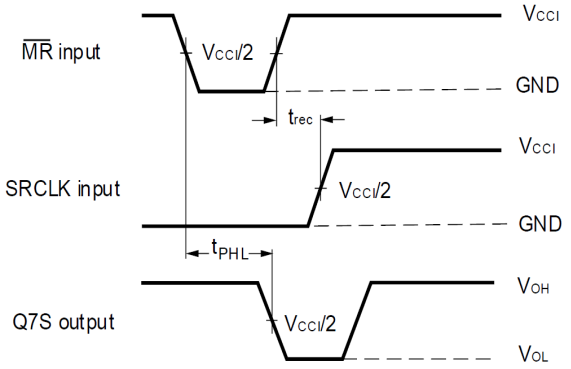


Figure 4. Master Reset to Output Propagation Delays

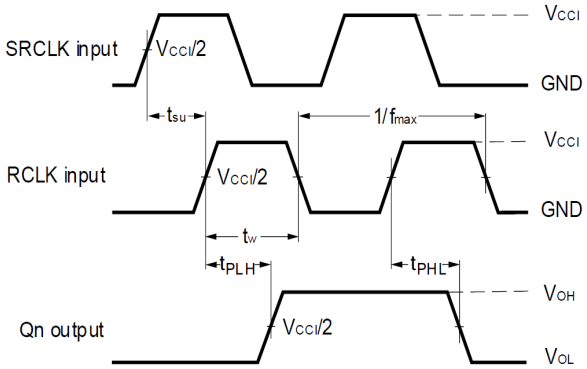


Figure 5. Storage Clock to Output Propagation Delays

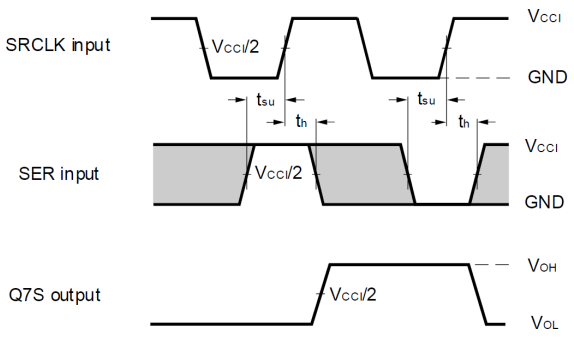


Figure 6. Data Set-up and Hold Times

NOTE:

A: C_L includes probe and jig capacitance.

B: All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, ZO = 50Ω , dv/dt≥1V/ns.

C: The outputs are measured one at a time, with one transition per measurement.

D: t_{PLZ} and t_{PHZ} are the same as t_{dis}.

E: t_{PZL} and t_{PZH} are the same as t_{en}.

F: t_{PLH} and t_{PHL} are the same as t_{pd}.

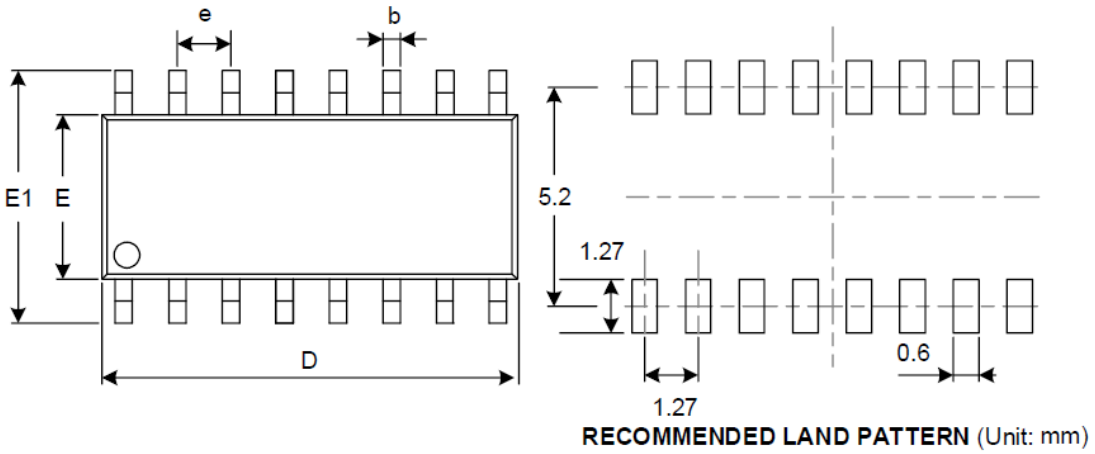
G: All parameters and waveforms are not applicable to all devices.

H: The shaded areas indicate when the input is permitted to change for predictable output performance.

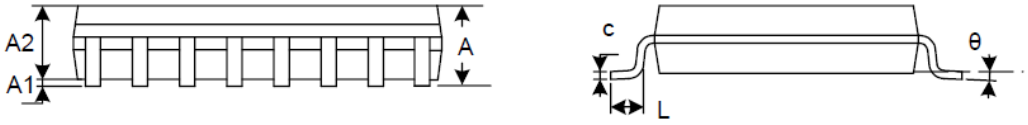
I: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

PACKAGE INFORMATION

Dimension in SOP16 (Unit: mm)

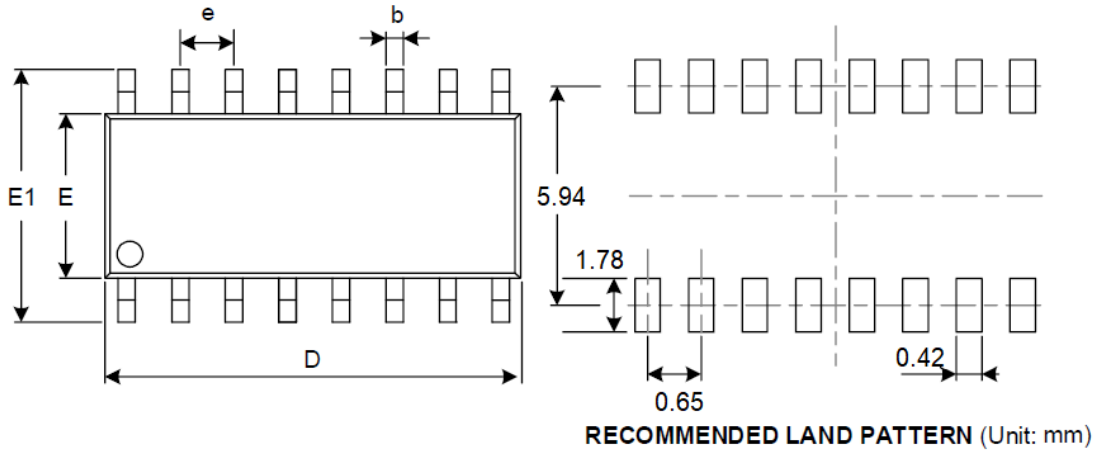


RECOMMENDED LAND PATTERN (Unit: mm)

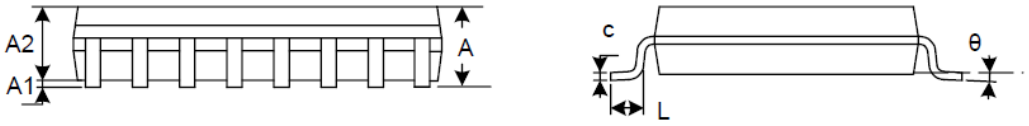


Symbol	Min.	Max.
A	-	1.750
A1	0.100	0.225
A2	1.300	1.500
b	0.390	0.470
c	0.200	0.240
D	9.800	10.000
E	3.800	4.000
E1	5.800	6.200
e	1.270 BSC	
L	0.500	0.800
θ	0°	8°

Dimension in TSSOP16 Package (Unit: mm)

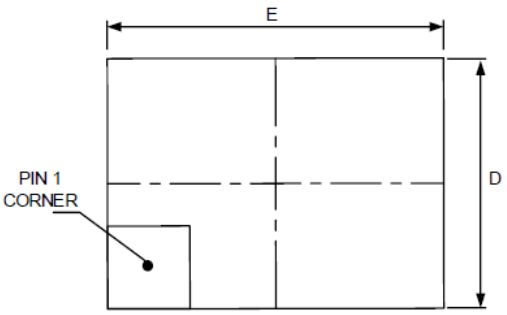


RECOMMENDED LAND PATTERN (Unit: mm)

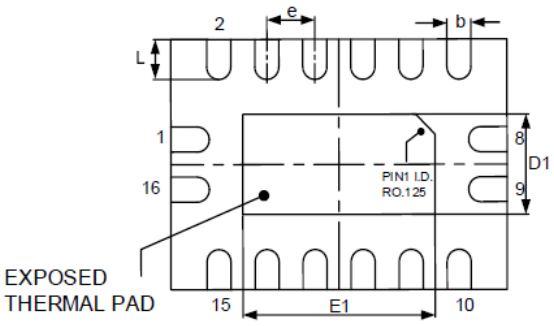


Symbol	Min.	Max.
A	-	1.200
A1	0.050	0.150
A2	0.900	1.050
b	0.200	0.280
c	0.130	0.170
D	4.900	5.100
E	4.300	4.500
E1	6.200	6.600
e	0.650 BSC	
L	0.450	0.750
θ	0°	8°

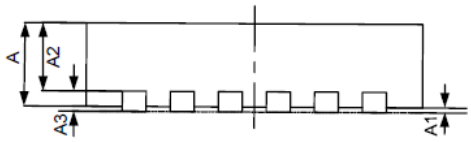
Dimension in QFN16 (2.5X3.5) (Unit: mm)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Min	Max
A	0.700	0.800
A1	0.000	0.050
A2	0.600	0.700
A3	0.203 REF	
D	2.400	2.600
E	3.400	3.600
e	0.500 BSC	
b	0.200	0.300
L	0.300	0.500
D1	0.850	1.150
E1	1.850	2.150

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