



DESCRIPTION

A24C64A provides 65536 bits of serial electrically erasable and programmable read-only memory (EEPROM), organized as 8192 bytes.

The A24C64A is optimized for use in many industrial and commercial applications where low-power and low-voltage operation is essential.

A24C64A offers an additional page, named the Identification Page (32 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

The A24C64A is available in SOP8, TSSOP8, DFN8, SOT-25 and TSOT-25 packages.

AEC-Q100 Qualified is available in SOP8, TSSOP8 and DFN8 packages.

ORDERING INFORMATION

Package Type	Part Number	
SOP8 AEC-Q100 SPQ: 2,500pcs/Reel	M8	A24C64AM8VR-X
TSSOP8 AEC-Q100 SPQ: 3,000pcs/Reel	TMX8	A24C64ATMX8VR-X
DFN8 AEC-Q100 SPQ: 3,000pcs/Reel	J8	A24C64AJ8VR-X
SOT-25 SPQ: 3,000pcs/Reel	E5	A24C64AE5VR-X
TSOT-25 SPQ: 3,000pcs/Reel	TE5	A24C64ATE5VR-X
Note	X: Temperature, AEC-Q B : -40°C to +105°C C : -40°C to +125°C Q : AEC-Q100 V: Halogen Free Package R: Tape & Reel	
AiT provides all RoHS products		

FEATURES

- Compatible with all I²C bidirectional data transfer protocol
- Memory Array:
64 Kbits (8192X8) of EEPROM
Page size: 32 bytes
Additional Write lockable page
- Extended Temperature Range
B : -40°C to +105°C
C : -40°C to +125°C
Q : -40°C to +125°C (AEC-Q100 Certificated)
- Single Supply Voltage and High Speed:
1.7V-5.5V ,1MHz
Random and sequential Read modes
- Write:
Byte Write within 3 ms
Page Write within 3 ms
Partial Page Writes Allowed
- Write Protect Pin for Hardware Data Protection
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- High-Reliability
Endurance: 1 Million Write Cycles
Data Retention: 100 Years
- Enhanced ESD/Latch-up Protection
HBM 8000V



PIN DESCRIPTION

<p style="text-align: center;">A24C64A SOP8</p> <p style="text-align: center;">SOP8, M8 Top View</p>	<p style="text-align: center;">A24C64A TSSOP8</p> <p style="text-align: center;">TSSOP8, TMX8 Top View</p>	<p style="text-align: center;">A24C64A DFN8</p> <p style="text-align: center;">DFN8, J8 Top View</p>		
<p style="text-align: center;">A24C64A SOT-25</p> <p style="text-align: center;">SOT-25, E5 Top View</p>	<p style="text-align: center;">A24C64A TSOT-25</p> <p style="text-align: center;">TSOT-25, TE5 Top View</p>			
Pin #		Symbol	Type	Functions
SOP8 / TSSOP8 DFN8	SOT-25 TSOT-25			
1,2,3	-	A0-A2	I	Address Inputs
4	2	GND	P	Ground
5	3	SDA	I/O	Serial Data
6	1	SCL	I	Serial Clock Input
7	5	WP	I	Write Protect
8	4	Vcc	P	Power Supply



ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	-0.3V ~ +6.5V
Input / Output Voltage	GND-0.3V ~ V _{CC} +0.3V
Storage Temperature	-65°C ~ +150°C
Electrostatic Pulse (Human Body Model)	8000V

Stresses above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CAPACITANCE

Applicable over recommended operating range from: T_A = 25°C, f = 1.0MHz, V_{CC} = +2.5V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input/ Output Capacitance (SDA)	C _{I/O}	V _{I/O} =0V	-	-	8	pF
Input Capacitance (A0, A1, A2, SCL)	C _{IN}	V _{IN} =0V	-	-	6	pF

DC ELECTRICAL CHARACTERISTICS

Applicable over recommended operating range, unless otherwise noted

A24C64A-B	T _A = -40°C to +105°C	V _{CC} = +1.7V to +5.5V@400kHz V _{CC} = +2.5V to +5.5V@1MHz C _L =100 pF
A24C64A-C	T _A = -40°C to +125°C	
A24C64A-Q	T _A = -40°C to +125°C	

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current V _{CC} = 5.0V	I _{CCR}	Read at 400kHz	-	0.14	0.3	mA
Supply Current V _{CC} = 5.0V	I _{CCW}	Write at 400kHz	-	0.28	0.5	mA
Supply Current V _{CC} = 5.0V	I _{SB}	V _{IN} = V _{CC} or GND	-	0.03	2.0	μA
Input Leakage Current	I _{LI}	V _{IN} = V _{CC} or GND	-	0.10	1.0	μA
Output Leakage Current	I _{LO}	V _{OUT} = V _{CC} or V _{SS}	-	0.05	1.0	μA
Input Low Level	V _{IL}	V _{CC} = 1.7V to 5.5V	-0.3	-	V _{CC} x 0.3	V
Input High Level	V _{IH}	V _{CC} = 1.7V to 5.5V	V _{CC} x0.7	-	V _{CC} + 0.3	V
Output Low Level V _{CC} = 1.7V	V _{OL1}	I _{OL} = 0.15mA	-	-	0.2	V
Output Low Level V _{CC} = 5.0V	V _{OL2}	I _{OL} = 3.0mA	-	-	0.4	V



AC ELECTRICAL CHARACTERISTICS (2)

Applicable over recommended operating range, unless otherwise noted

A24C64A-B	T _A = -40°C to +105°C	V _{CC} = +1.7V to +5.5V@400kHz
A24C64A-C	T _A = -40°C to +125°C	
A24C64A-Q	T _A = -40°C to +125°C	V _{CC} = +2.5V to +5.5V@1MHz
		C _L = 100 pF

Parameter	Symbol	1.7V ≤ V _{CC} < 2.5V			2.5V ≤ V _{CC} < 5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency, SCL	f _{SCL}	-	-	400	-	-	1000	kHz
Clock Pulse Width Low	t _{LOW}	1.3	-	-	0.5	-	-	µs
Clock Pulse Width High	t _{HIGH}	0.6	-	-	0.26	-	-	µs
Noise Suppression Time	t _i	-	-	50	-	-	50	ns
Clock Low to Data Out Valid	t _{AA}	-	-	0.9	-	-	0.45	µs
Time the bus must be free before a new transmission can start	t _{BUF}	1.3	-	-	0.5	-	-	µs
Start Hold Time	t _{HD,STA}	0.6	-	-	0.25	-	-	µs
Start Setup Time	t _{SU,STA}	0.6	-	-	0.25	-	-	µs
Data In Hold Time	t _{HD,DAT}	0	-	-	0	-	-	µs
Data In Setup Time	t _{SU,DAT}	100	-	-	100	-	-	ns
Inputs Rise Time (1)	t _R	-	-	0.3	-	-	0.12	µs
Inputs Fall Time (1)	t _F	-	-	0.3	-	-	0.12	µs
Stop Setup Time	t _{SU,STO}	0.6	-	-	0.25	-	-	µs
Data Out Hold Time	t _{DH}	50	-	-	50	-	-	ns
Write Cycle Time	t _{WR}	-	1.9	3	-	1.9	3	ms
5.0V, 25°C, Byte Mode (1)	Endurance	1M	-	-	1M	-	-	Write Cycles

(1): This parameter is characterized and is not 100% tested.

(2): AC measurement conditions: R_L(connects to V_{CC}): 1.3K

Input pulse voltages: 0.3 V_{CC} to 0.7V_{CC}

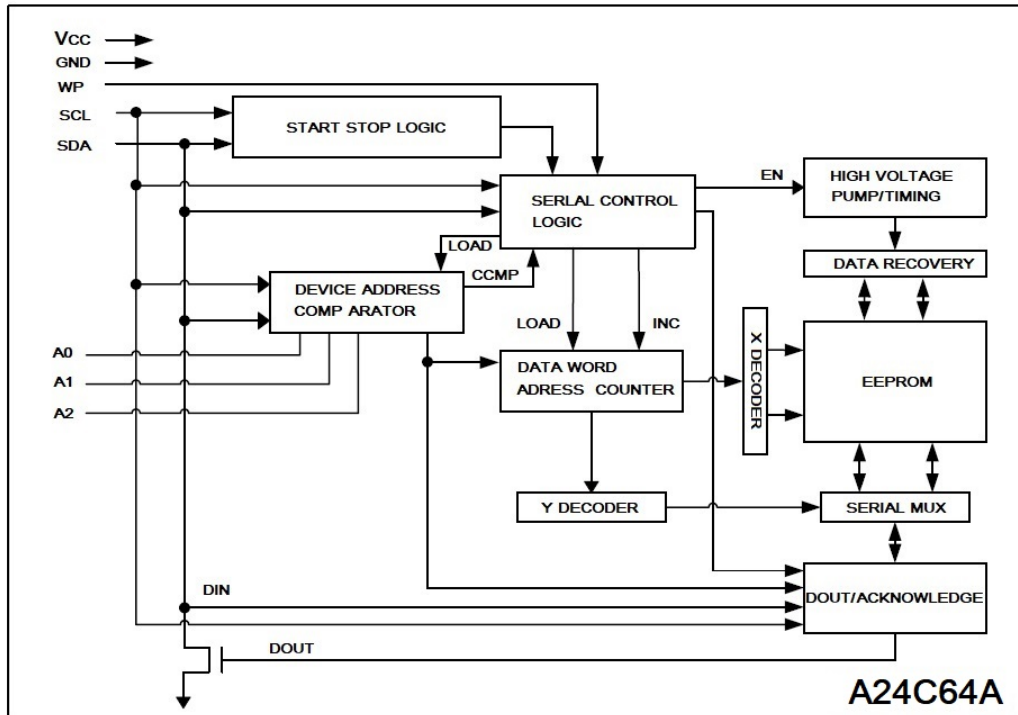
Input rise and fall time: 50ns

Input and output timing reference voltages: 0.5V_{CC}

The value of R_L should be concerned according to the actual loading on the user's system.



BLOCK DIAGRAM





DETAILED INFORMATION

DEVICE/PAGE ADDRESSES (A2, A1 and A0): The A2, A1 and A0 pins are device address inputs that are hard wire for the A24C64A. Eight 32K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-OR 'ed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

WRITE PROTECT (WP): The A24C64A has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protection pin is connected to V_{CC} , the write protection feature is enabled and operates as shown in the following Table 1.

Table1: Write Protect

WP Pin Status	A24C64A
At V_{CC}	Full (64K) Array
At GND	Normal Read/Write Operations



FUNCTION DESCRIPTION

1. Memory Organization

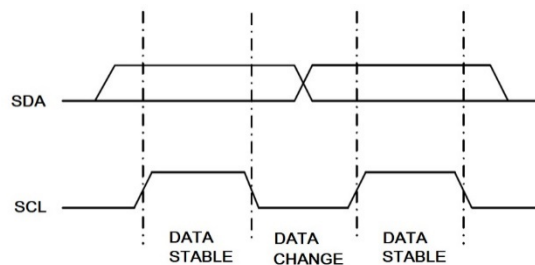
A24C64A, 64K SERIAL EEPROM: Internally organized with 256 pages of 32 bytes each, the 64K requires a 13-bit data word address for random word addressing.

2. Device Operation

CLOCK and DATA TRANSITIONS:

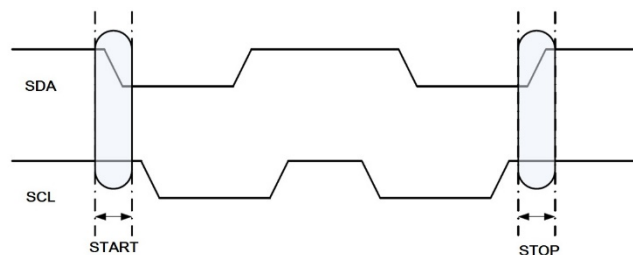
The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 1). Data changes during SCL high periods will indicate a start or stop condition as defined.

Figure 1 Data Validity



START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 2).

Figure 2 Start and Stop Definition

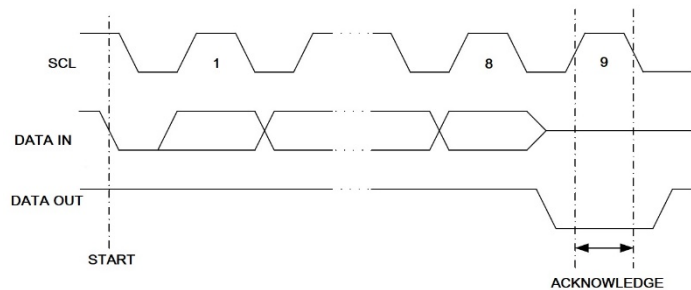


STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. (see Figure 2).

ACKNOWLEDGE:

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle.

Figure 3 Output Acknowledge



STANDBY MODE: The A24C64A features a low-power standby mode which is enabled:

- (a) Upon power-up
- (b) After the receipt of the STOP bit and the completion of any internal operations.



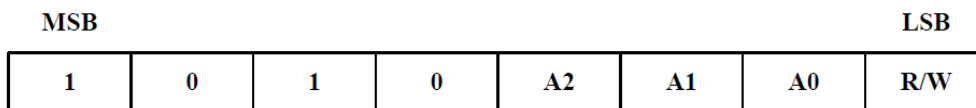
MEMORY RESET: After the protocol is interrupted, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition and a stop condition.

3. Device Addressing

The 64K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 4).

Figure 4 Device Address



The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 64K EEPROM uses A2, A1 and A0 device address bits to allow as much as eight devices on the same bus. These 3 bits must be compared to their corresponding hardwired input pins. The A2, A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

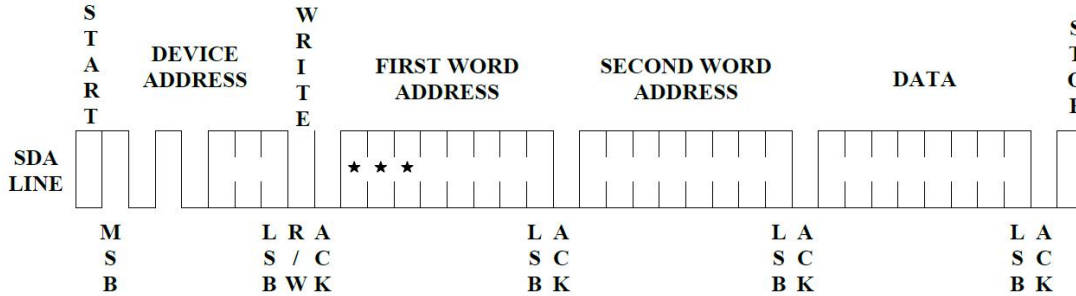
DATA SECURITY: The A24C64A has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}.

4. Write Operations

BYTE WRITE: A write operation requires two 8-bit data word address (see Table 2 & Table 3) following the device address word and acknowledgment. Upon receipt of every 8-bit address, the EEPROM will respond with a "0" and then send 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the master device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, in order to save the data in the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5).



Figure 5 Byte Write



Note.1*=DON'T CARE bits

Table2: FIRST WORD ADDRESS

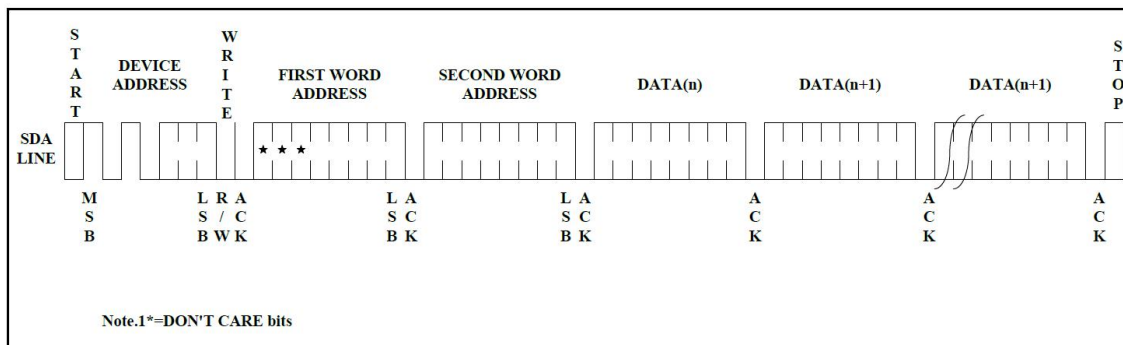
B15	B14	B13	B12	B11	B10	B9	B8
-----	-----	-----	-----	-----	-----	----	----

Table3: SECOND WORD ADDRESS

B7	B6	B5	B4	B3	B2	B1	B0
----	----	----	----	----	----	----	----

PAGE WRITE: The Page Write mode allows up to 32 bytes to be written in a single Write cycle. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 31 more data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6).

Figure 6 Page Write



Note.1*=DON'T CARE bits

The data word address lower four bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than thirty-two data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.



WRITE IDENTIFICATION PAGE: The identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. It is written by issuing the Write Identification Page instruction. This instruction uses the same protocol and format as Page Write (into memory array), except for the following differences: Device type identifier = 1011b

MSB address bits B15/B5 are don't care except for address bit B10 which must be "0".

LSB address bits B4/B0 define the byte address inside the Identification page.

If the Identification page is locked, the data bytes transferred during the Write Identification Page instruction are not acknowledged (NoAck).

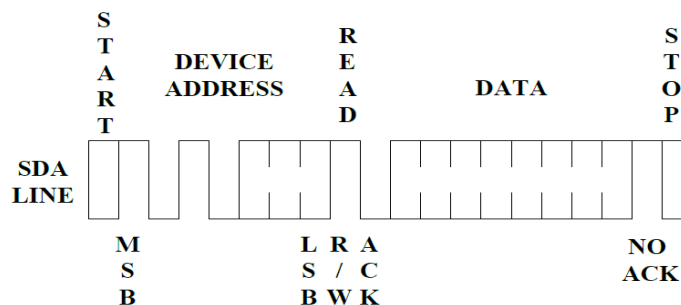
ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

5.Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page. Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7).

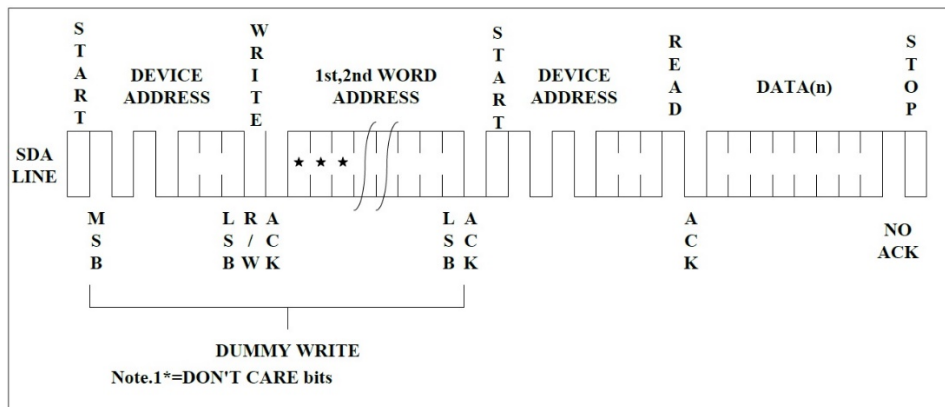
Figure 7 Current Address Read





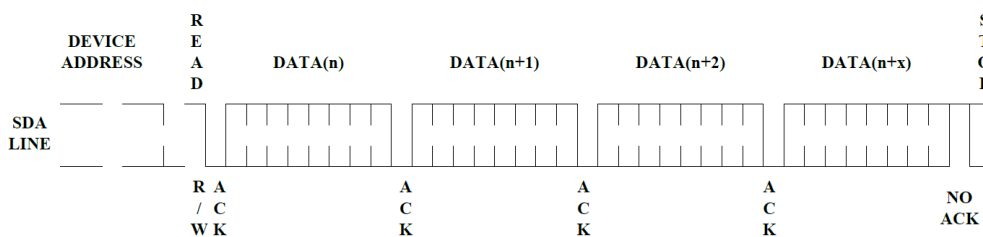
RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 8)

Figure 8 Random Read



SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 9).

Figure 9 Sequential Read



READ IDENTIFICATION PAGE: The Identification Page (32 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

The Identification Page can be read by issuing a Read Identification Page instruction. This instruction uses the same protocol and format as the Random Address Read (from memory array) with device type identifier defined as 1011b. The MSB address bits B15/B6 are don't care, the LSB address bits B4/B0 define the byte address inside the identification Page. The number of bytes to read in the ID page must not exceed the page



boundary (e.g. when reading the identification Page from location 10d, the number of bytes should be less than or equal to 22, as the ID page boundary is 32 bytes)

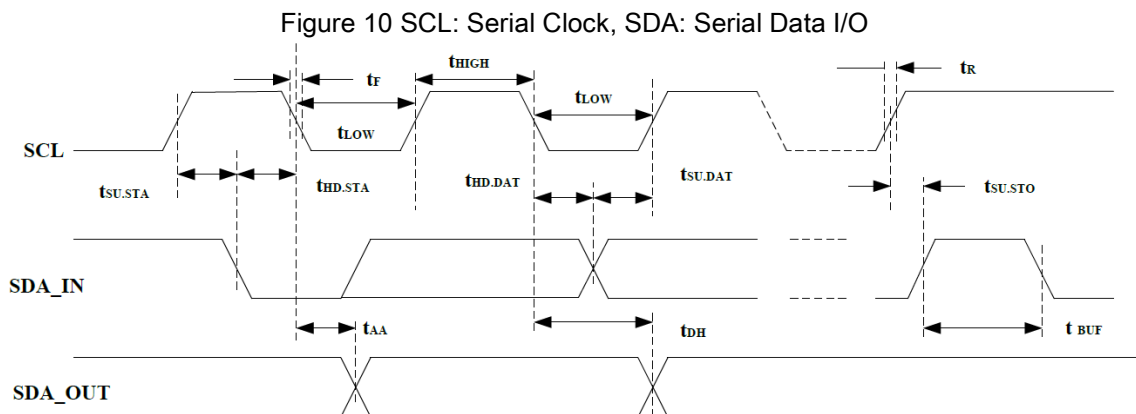
LOCK IDENTIFICATION PAGE: The Lock Identification Page instruction (Lock ID) permanently locks the Identification page in Read-only mode. The Lock ID instruction is similar to Byte Write (into memory array) with the following specific conditions:

Device type identifier = 1011b

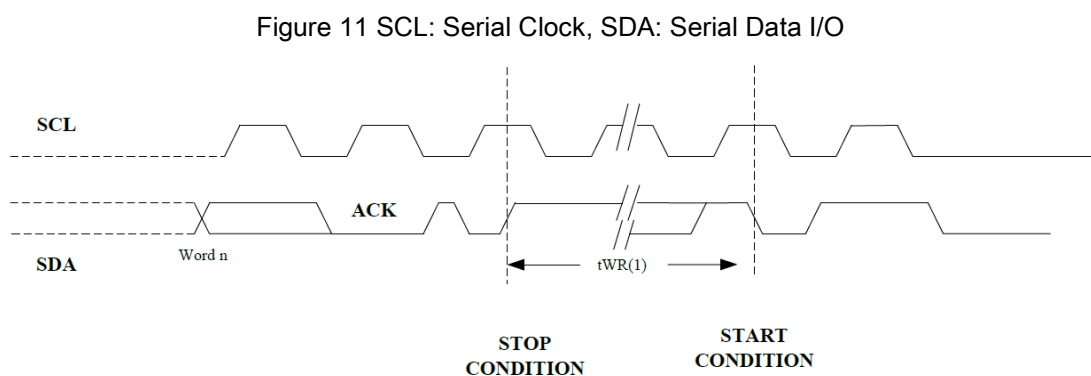
Address bit B10 must be "1"; all other address bits are don't care

The data byte must be equal to the binary value xxxx xx1x, where x is don't care

BUS TIMING



WRITE CYCLE TIMING

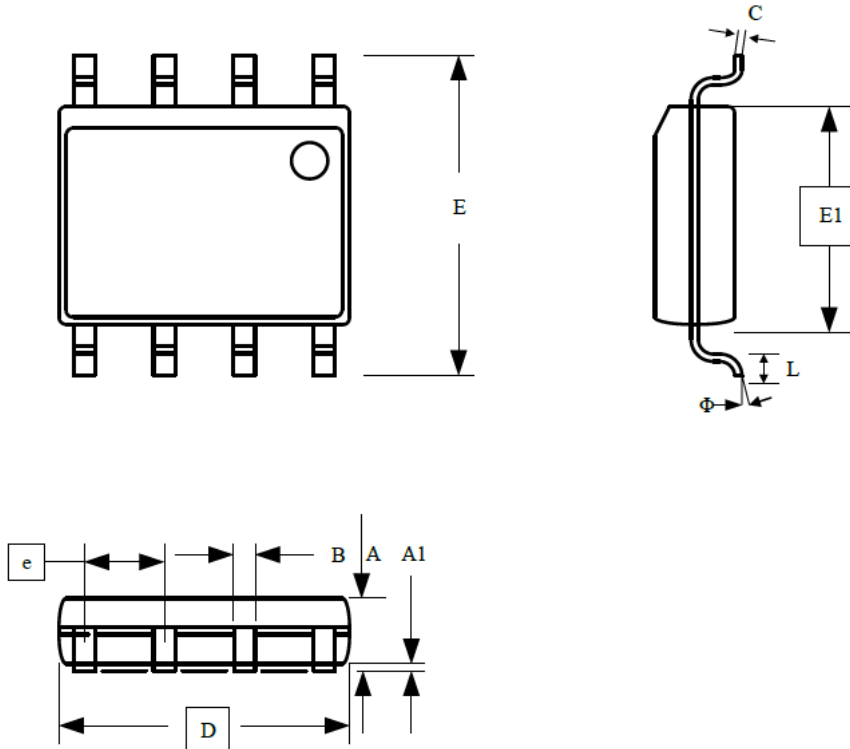


NOTE: The write cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.



PACKAGE INFORMATION

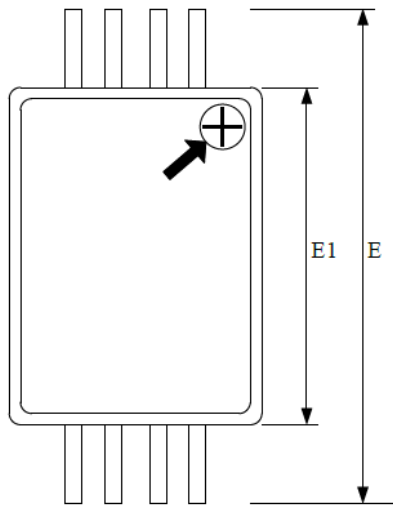
Dimension in SOP8 (Unit: mm)



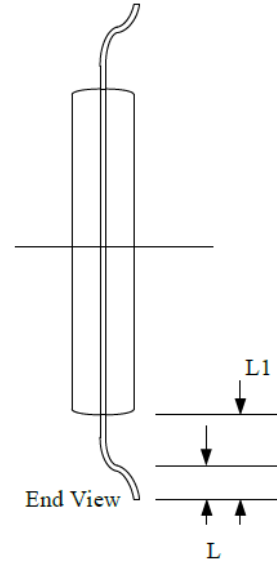
Symbol	Min	Max
A	1.350	1.750
A1	0.100	0.230
B	0.390	0.480
C	0.210	0.260
D	4.700	5.100
E1	3.700	4.100
E	5.800	6.200
e	1.27BSC	
L	0.500	0.800
θ	0°	8°



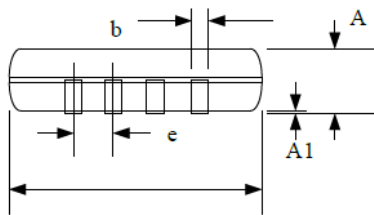
Dimension in TSSOP8 Package (Unit: mm)



Top View



End View

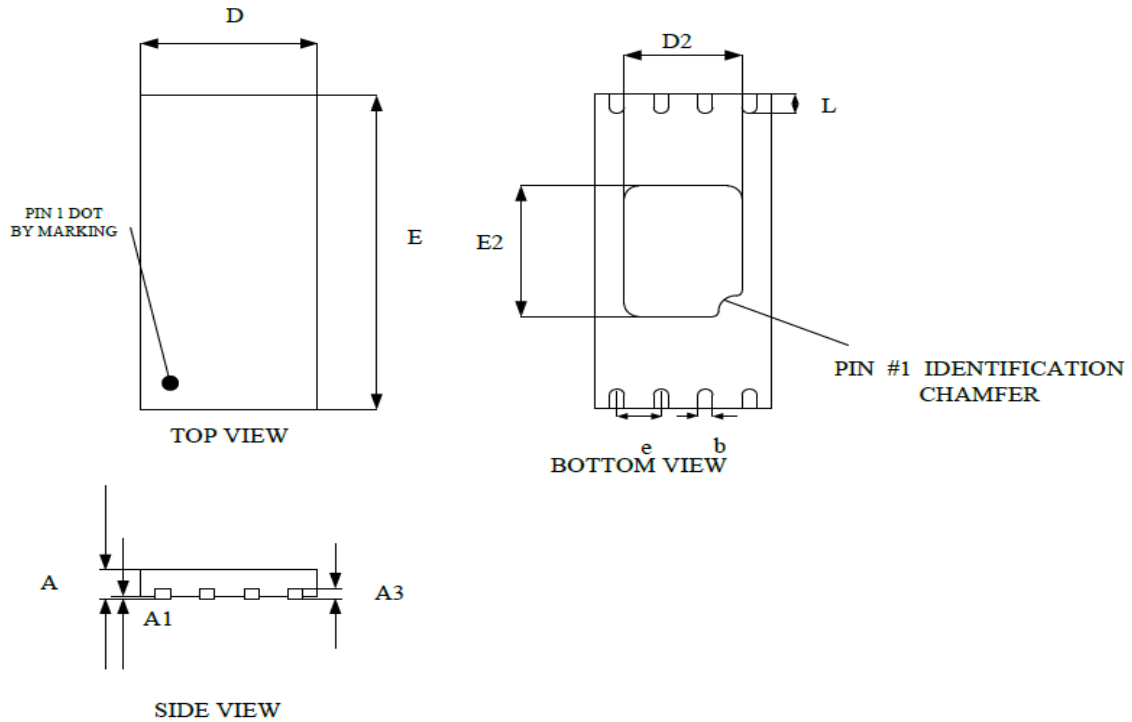


Side View

Symbol	Min	Max
D	2.900	3.100
E	6.200	6.600
E1	4.300	4.500
A	-	1.200
A1	0.050	0.150
b	0.210	0.300
e	0.650 BSC	
L	0.450	0.750
L1	1.000 REF	



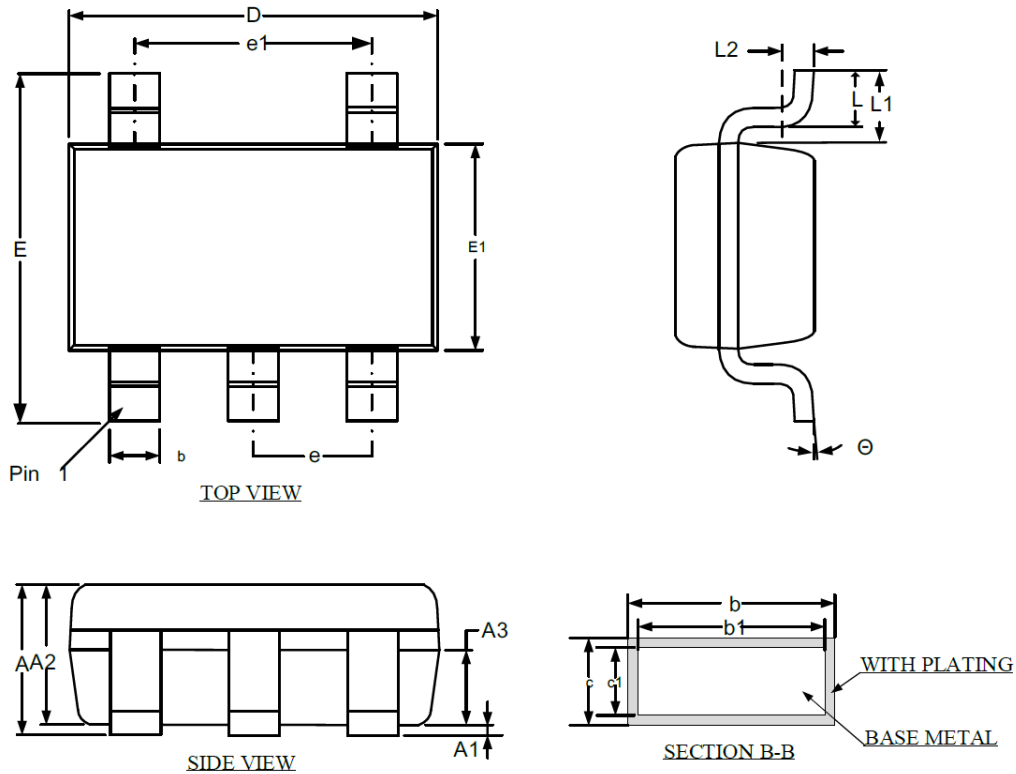
Dimension in DFN8 (Unit: mm)



Symbol	Min	Max
A	0.500	0.600
A1	0.000	0.050
A3	0.15 REF	
D	1.950	2.050
E	2.950	3.050
b	0.200	0.300
L	0.200	0.400
D2	1.250	1.500
E2	1.150	1.400
e	0.500 BSC	



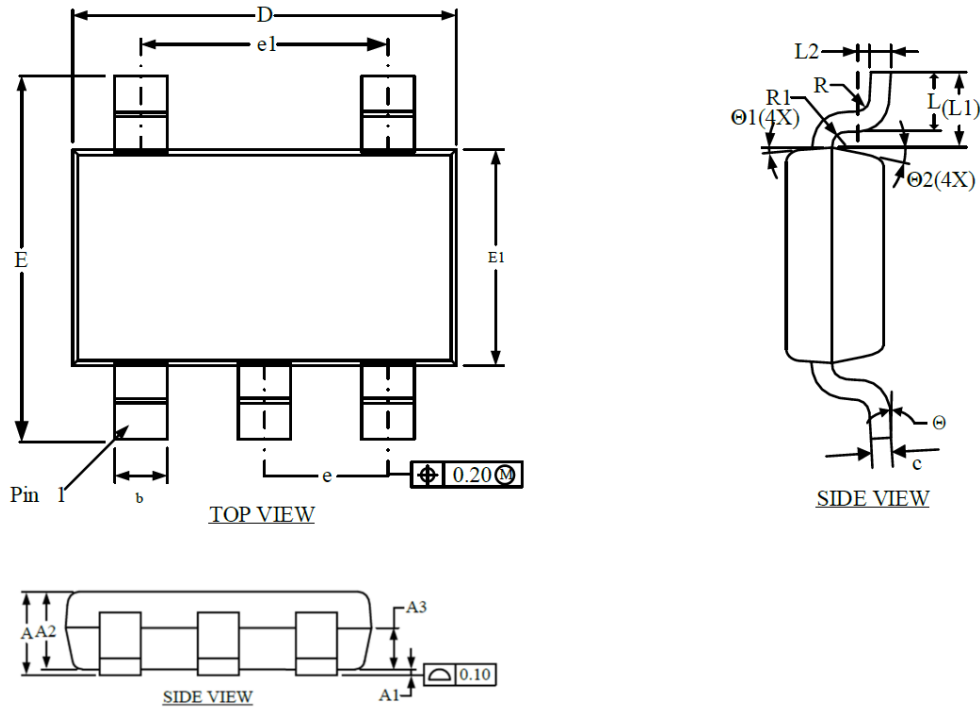
Dimension in SOT-25 (Unit: mm)



Symbol	Min.	Max.
A	-	1.350
A1	0.040	0.150
A2	1.000	1.200
A3	0.550	0.750
b	0.380	0.480
b1	0.370	0.430
c	0.110	0.210
c1	0.100	0.160
D	2.720	3.120
E	2.600	3.000
E1	1.400	1.800
e	0.950 BSC	
e1	1.900 BSC	
L	0.300	0.600
L1	0.575 REF	
L2	0.258 BSC	
θ	0°	8°



Dimension in TSOT-25 (Unit: mm)



Symbol	Min	Max
A	-	0.900
A1	0.000	0.100
A2	0.650	0.850
A3	0.350	0.450
b	0.300	0.500
c	0.140	0.200
D	2.850	3.050
E	2.650	2.950
E1	1.600	1.700
e	0.900	1.000
e1	1.800	2.000
L	0.300	0.600
L1	0.575 REF	
L2	0.258 BSC	
R	-	0.25
R1	-	0.25
theta	0°	8°
theta1	3°	7°
theta2	10°	14°



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