



## DESCRIPTION

The A25C64 devices are Electrically Erasable Programmable Memory (EEPROM) organized as 8192 x 8 bits, accessed through the SPI bus.

The A25C64 can operate with a supply range from 1.7V to 5.5V

The A25C64 is available in SOP8, TSSOP8 and DFN8, packages.

## ORDERING INFORMATION

Package Type	Part Number	
SOP8 SPQ:2,500pcs/Reel	M8	A25C64M8R-X
		A25C64M8VR-X
TSSOP8 SPQ: 3,000pcs/Reel	TMX8	A25C64TMX8R-X
		A25C64TMX8VR-X
DFN8 SPQ: 3,000pcs/Reel	J8	A25C64J8R-X
		A25C64J8VR-X
Note	X: Temperature A : -40°C to +85°C B : -40°C to +105°C C : -40°C to +125°C V: Halogen Free Package R: Tape & Reel	
AiT provides all RoHS products		

## FEATURES

- Serial Peripheral Interface (SPI) data transfer Protocol  
Memory A25C64:  
64 Kbits (8 Kbytes) of EEPROM  
Page size: 32 bytes
- Extended Temperature Range  
A : -40°C to +85°C  
B : -40°C to +105°C  
C : -40°C to +125°C
- Single Supply Voltage and High Speed:  
V<sub>CC</sub> ≥ 1.7 V 5MHz  
V<sub>CC</sub> ≥ 2.5 V 10MHz  
V<sub>CC</sub> ≥ 4.5 V 20MHz
- Random and sequential Read modes
- Write:  
Write within 3 ms  
Partial Page Writes Allowed
- Write Protect: Quarter, Half or Whole Memory Array
- High-Reliability  
Endurance: 4 Million Write Cycles  
Data Retention: 100 Years
- Enhanced ESD/Latch-up Protection  
HBM 4000V



**PIN DESCRIPTION**

<p><b>A25C64 SOP8</b> SOP8, M8 Top View</p>	<p><b>A25C64 TSSOP8</b> TSSOP8, TMX8 Top View</p>	<p><b>A25C64 DFN8</b> DFN8, J8 Top View</p>	
Pin #	Symbol	Type	Functions
<b>SOP8 / TSSOP8 / DFN8</b>			
1	$\overline{CS}$	I	Chip Select
2	SO	O	Serial Data Output
3	$\overline{WP}$	I	Write Protect
4	V <sub>SS</sub>	P	Ground
5	SI	I	Serial Data Input
6	SCK	I	Serial Clock
7	$\overline{HOLD}$	I	Hold
8	V <sub>CC</sub>	P	Power Supply

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature	-65°C ~ +150°C
Voltage on any Pin with Respect to Ground *	-0.5V ~ +6.5V
V <sub>ESD</sub> (HBM)	4000V

Stresses above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

\*The DC input voltage on any pin should not be lower than -0.5 V or higher than V<sub>CC</sub> + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than V<sub>CC</sub> + 1.5 V, for periods of less than 20 ns.



## RELIABILITY CHARACTERISTICS (2)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	$N_{END}^{(1)(2)}$	4000000	-	-	Program/Erase Cycles
Data Retention	$T_{DR}$	100	-	-	Years

(1) Page Mode,  $V_{CC} = 5\text{ V}$ ,  $25^{\circ}\text{C}$ .

(2) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

## DC ELECTRICAL CHARACTERISTICS

$V_{CC} = 1.7\text{ V}$  to  $5.5\text{ V}$ , unless otherwise specified.

A25C64-A	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	$V_{CC} = +1.7\text{V}$ to $+5.5\text{V}$
A25C64-B	$T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$	
A25C64-C	$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Current (Read Mode)	$I_{CCR}$	Read, SO open $1.7\text{ V} < V_{CC} < 5.5\text{ V}$	-	-	3	mA
Supply Current (Write Mode)	$I_{CCW}$	Write, $\overline{CS} = V_{CC}$ $1.7\text{ V} < V_{CC} < 5.5\text{ V}$	-	-	3	mA
Standby Current	$I_{SB1}^*$	$V_{IN} = \text{GND}$ or $V_{CC}$ , $\overline{CS} = V_{CC}$ , $\overline{WP} = V_{CC}$ , $\overline{HOLD} = V_{CC}$ , $V_{CC} = 5.5\text{ V}$	-	-	5	$\mu\text{A}$
Standby Current	$I_{SB2}^*$	$V_{IN} = \text{GND}$ or $V_{CC}$ , $\overline{CS} = V_{CC}$ , $\overline{WP} = \text{GND}$ , $\overline{HOLD} = \text{GND}$ , $V_{CC} = 5.5\text{ V}$	-	-	5	$\mu\text{A}$
Input Leakage Current	$I_L$	$V_{IN} = \text{GND}$ or $V_{CC}$	-	-	$\pm 2$	$\mu\text{A}$
Output Leakage Current	$I_{LO}$	$\overline{CS} = V_{CC}$ , $V_{OUT} = \text{GND}$ or $V_{CC}$	-	-	$\pm 2$	$\mu\text{A}$
Input Low Voltage	$V_{IL1}$	$V_{CC} \geq 1.7\text{ V}$	-0.45	-	$0.3 V_{CC}$	V
Input High Voltage	$V_{IH1}$	$V_{CC} \geq 1.7\text{ V}$	$0.7 V_{CC}$	-	$V_{CC} + 1$	V
Output Low Voltage	$V_{OL1}$	$V_{CC} \geq 1.7\text{ V}$ , $I_{OL} = 3.0\text{ mA}$	-	-	0.4	V
Output High Voltage	$V_{OH1}$	$V_{CC} \geq 1.7\text{ V}$ , $I_{OH} = -1.6\text{ mA}$	$0.8 V_{CC}$	-	-	V

\* AC Test Conditions: (1) Input Pulse Voltages:  $0.3 V_{CC}$  to  $0.7 V_{CC}$  (2) Input rise and fall times:  $\leq 10\text{ ns}$

(3) Input and output reference voltages:  $0.5 V_{CC}$  (4) Output load: current source  $I_{OL\text{ max}}/I_{OH\text{ max}}$ ;  $C_L = 30\text{ pF}$



**AC ELECTRICAL CHARACTERISTICS (1)**

V<sub>CC</sub> = 1.7 V to 5.5 V, unless otherwise specified.

A25C64-A	T <sub>A</sub> = -40°C to +85°C	V <sub>CC</sub> = +1.7V to +5.5V
A25C64-B	T <sub>A</sub> = -40°C to +105°C	
A25C64-C	T <sub>A</sub> = -40°C to +125°C	

Parameter	Symbol	V <sub>CC</sub> > 1.7 V			V <sub>CC</sub> > 2.5 V			V <sub>CC</sub> > 4.5 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	f <sub>SCK</sub>	DC	-	5	DC	-	10	DC	-	20	MHz
Data Setup Time	t <sub>SU</sub>	20	-	-	10	-	-	5	-	-	ns
Data Hold Time	t <sub>H</sub>	20	-	-	10	-	-	5	-	-	ns
SCK High Time	t <sub>WH</sub>	80	-	-	40	-	-	20	-	-	ns
SCK Low Time	t <sub>WL</sub>	80	-	-	40	-	-	20	-	-	ns
HOLD to Output Low Z	t <sub>LZ</sub>	-	-	80	-	-	40	-	-	25	ns
Input Rise Time	t <sub>RI</sub> (2)	-	-	1	-	-	1	-	-	1	μs
Input Fall Time	t <sub>FI</sub> (2)	-	-	1	-	-	1	-	-	1	μs
HOLD Setup Time	t <sub>HD</sub>	0	-	-	0	-	-	0	-	-	ns
HOLD Hold Time	t <sub>CD</sub>	20	-	-	10	-	-	5	-	-	ns
Output Valid from Clock Low	t <sub>V</sub>	-	-	80	-	-	40	-	-	20	ns
Output Hold Time	t <sub>HO</sub>	0	-	-	0	-	-	0	-	-	ns
Output Disable Time	t <sub>DIS</sub>	-	-	80	-	-	40	-	-	20	ns
HOLD to Output High Z	t <sub>HZ</sub>	-	-	80	-	-	40	-	-	20	ns
CS High Time	t <sub>CS</sub>	80	-	-	50	-	-	25	-	-	ns
CS Setup Time	t <sub>CSS</sub>	20	-	-	10	-	-	5	-	-	ns
CS Hold Time	t <sub>CSH</sub>	100	-	-	50	-	-	25	-	-	ns
CS Inactive Setup Time	t <sub>CNS</sub>	60	-	-	30	-	-	15	-	-	ns
CS Inactive Hold Time	t <sub>CNH</sub>	60	-	-	30	-	-	15	-	-	ns
WP Setup Time	t <sub>WPS</sub>	20	-	-	20	-	-	20	-	-	ns
WP Hold Time	t <sub>WPH</sub>	20	-	-	20	-	-	20	-	-	ns
Write Cycle Time	t <sub>WC</sub> (3)	-	-	3	-	-	3	-	-	3	ms

(1) AC Test Conditions:

Input Pulse Voltages: 0.3 V<sub>CC</sub> to 0.7 V<sub>CC</sub>

Input rise and fall times: ≤ 10 ns

Input and output reference voltages: 0.5 V<sub>CC</sub>

Output load: current source I<sub>OL</sub> max/I<sub>OH</sub> max; C<sub>L</sub> = 30 pF

(2) This parameter is tested initially and after a design or process change that affects the parameter.

(3) t<sub>WC</sub> is the time from the rising edge of CS after a valid write sequence to the end of the internal write cycle.

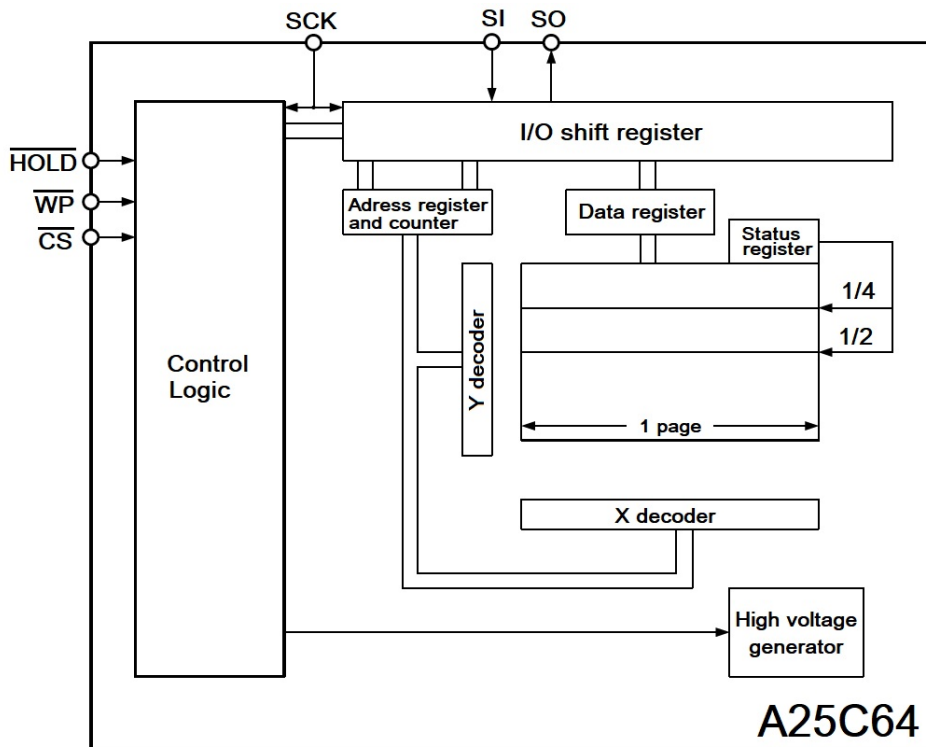


### POWER-UP TIMING <sup>(1)(2)</sup>

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power-up to Read	t <sub>PUR</sub>		-	-	0.1	ms
Write Operation	t <sub>PUW</sub>		-	-	0.1	ms

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) t<sub>PUR</sub> and t<sub>PUW</sub> are the delays required from the time V<sub>CC</sub> is stable until the specified operation can be initiated

### BLOCK DIAGRAM





## DETAILED INFORMATION

**Serial Data Input (SI):** The SPI Serial data input (SI) is used to serially receive write instructions, addresses or data to the device on the rising edge of the Serial Clock (SCK) input pin.

**Serial Data Output (SO):** The SPI Serial data output (SO) is used to read data or status from the device on the falling edge of CLK.

**Serial Clock (SCK):** The SPI Serial Clock Input (SCK) pin provides the timing for serial input and output operations.

**Chip Select ( $\overline{CS}$ ):** The SPI Chip Select ( $\overline{CS}$ ) pin enables and disables device operation. When ( $\overline{CS}$ ) is high, the device is deselected and the Serial Data Output (SO) pins are at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal write cycle is in progress. When ( $\overline{CS}$ ) is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, ( $\overline{CS}$ ) must transition from high to low before a new instruction will be accepted.

**Hold ( $\overline{HOLD}$ ):** The  $\overline{HOLD}$  pin allows the device to be paused while it is actively selected. When  $\overline{HOLD}$  is brought low, while  $\overline{CS}$  is low, the SO pin will be at high impedance and signals on the SI and SCK pins will be ignored (don't care). When  $\overline{HOLD}$  is brought high, device operation can resume. The  $\overline{HOLD}$  function can be useful when multiple devices are sharing the same SPI signals. The  $\overline{HOLD}$  pin is active low.

**Write Protect ( $\overline{WP}$ ):** The Write Protect ( $\overline{WP}$ ) pin is used in conjunction with the Status Register Write Disable (SRWD) Bit to prevent the Status Registers from being written. Write Protect ( $\overline{WP}$ ) pin and Status Register Write Disable (SRWD) Bit enable the device to be put in the Hardware Protected mode (when Status Register Write Disable (SRWD) Bit is set to 1, and Write Protect ( $\overline{WP}$ ) pin is driven low).



## FUNCTION DESCRIPTION

The A25C64 device supports the Serial Peripheral Interface (SPI) bus protocol, modes (0,0) and (1,1). The device contains an 8-bit instruction register. The instruction set and associated op-codes are listed in Table 1.

Reading data stored in the A25C64 is accomplished by simply providing the READ command and an address. Writing to the A25C64, in addition to a WRITE command, address and data, also requires enabling the device for writing by first setting certain bits in a Status Register, as will be explained later.

After a high to low transition on the  $\overline{CS}$  input pin, the A25C64 will accept any one of the six-instruction op-codes listed in Table 1 and will ignore all other possible 8-bit combinations. The communication protocol follows the timing from Figure 10.

Table 1

Instruction	Opcode	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory
WRITE	0000 0010	Write Data to Memory

### 1. Status Register

The Status Register, as shown in Table 2, contains a number of status and control bits.

Table 2

7	6	5	4	3	2	1	0
SRWD	0	0	0	BP1	BP0	WEL	$\overline{READY}$

**READY:** The  $\overline{READY}$  bit indicates whether the device is busy with a write operation. This bit is automatically set to 1 during an internal write cycle, and reset to 0 when the device is ready to accept commands. For the host, this bit is read only.

**BP0, BP1:** The BP0 and BP1 (Block Protect) bits determine which blocks are currently write protected. They are set by the user with the WRSR command and are non-volatile. The user is allowed to protect a quarter, one half or the entire memory, by setting these bits according to Table 3. The protected blocks then become read-only.



Table 3

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	1800h–1FFFh	Quarter Array Protection
1	0	1000h–1FFFh	Half Array Protection
1	1	0000h–1FFFh	Full Array Protection

**SRWD:** The SRWD (Status Register Write Disable) bit acts as an enable for the  $\overline{WP}$  pin. Hardware write protection is enabled when the  $\overline{WP}$  pin is low and the SRWD bit is 1. This condition prevents writing to the status register and to the block protected sections of memory. While hardware write protection is active, only the non-block protected memory can be written. Hardware write protection is disabled when the  $\overline{WP}$  pin is high or the SRWD bit is 0. The SRWD bit,  $\overline{WP}$  pin and WEL bit combine to either permit or inhibit Write operations, as detailed in Table 4.

Table 4

SRWD	$\overline{WP}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1	Protected	Writable	Writable

## 2. Write Operations

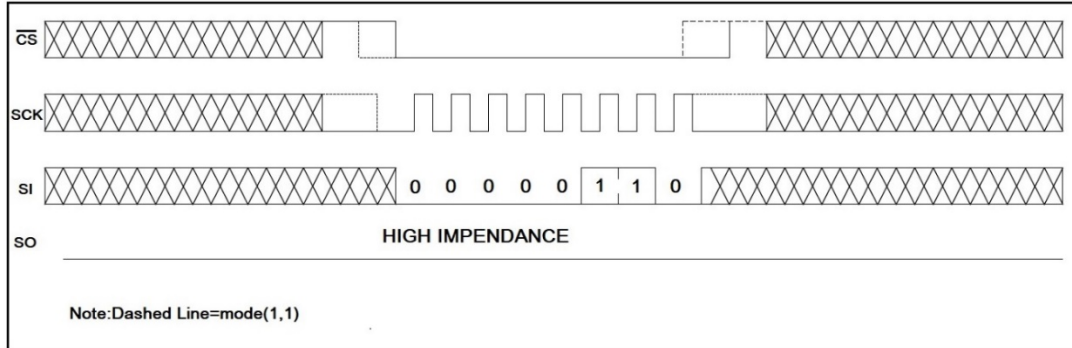
The A25C64 device powers up into a write disable state. The device contains a Write Enable Latch (WEL) which must be set before attempting to write to the memory array or to the status register. In addition, the address of the memory location(s) to be written must be outside the protected area, as defined by BP0 and BP1 bits from the status register.

**Write Enable and Write Disable:** The internal Write Enable Latch and the corresponding Status Register WEL bit are set by sending the WREN instruction to the A25C64. Care must be taken to take the  $\overline{CS}$  input high after the WREN instruction, as otherwise the Write Enable Latch will not be properly set. WREN timing is illustrated in Figure 1. The WREN instruction must be sent prior to any WRITE or WRSR instruction.



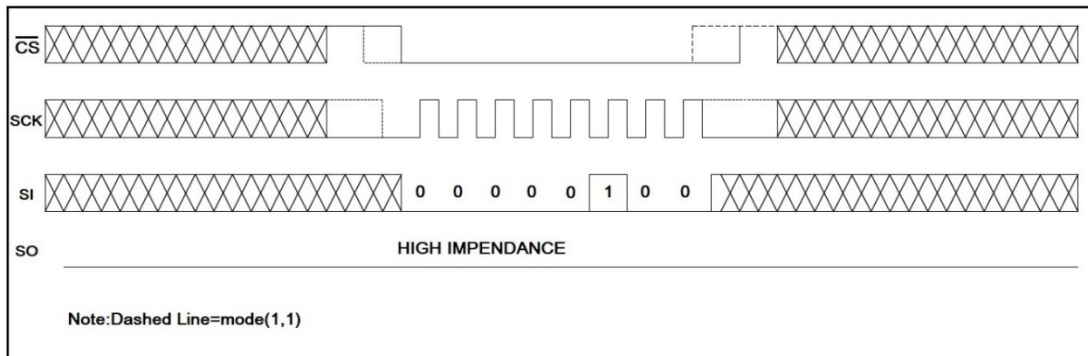


Figure 1



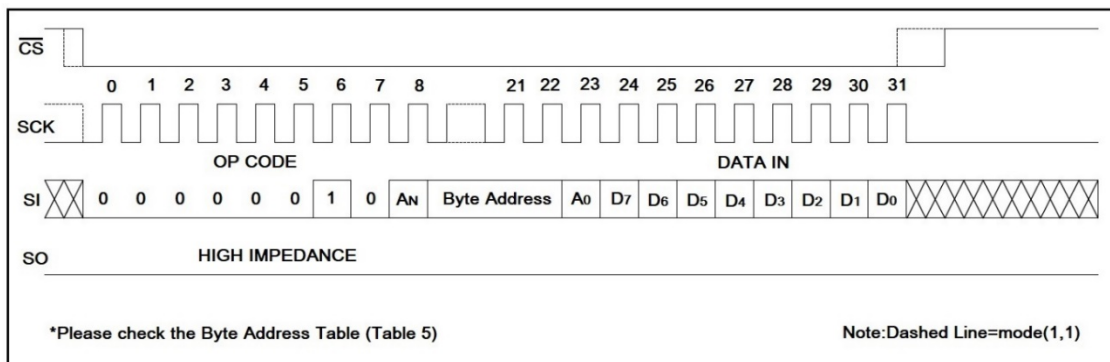
The internal write enable latch is reset by sending the WRDI instruction as shown in Figure 2. Disabling write operations by resetting the WEL bit, will protect the device against inadvertent writes.

Figure 2



**Byte Write:** Once the WEL bit is set, the user may execute a write sequence, by sending a WRITE instruction, a 16-bit address and a data byte as shown in Figure 3. Only 13 significant address bits are used by the A25C64. The rest are don't care bits. Internal programming will start after the low to high  $\overline{CS}$  transition. During an internal write cycle, all commands, except for RDSR (Read Status Register) will be ignored. The  $\overline{READY}$  bit will indicate if the internal write cycle is in progress ( $\overline{READY}$  high), or the device is ready to accept commands ( $\overline{READY}$  low).

Figure 3





**Page Write:** After sending the first data byte to the A25C64, the host may continue sending data, up to a total of 32 bytes, according to timing shown in Figure 4. After each data byte, the lower order address bits are automatically incremented, while the higher order address bits (page address) remain unchanged. If during this process the end of page is exceeded, then loading will “roll over” to the first byte in the page, thus possibly overwriting previously loaded data. Following completion of the write cycle, the A25C64 is automatically returned to the write disable state.

Figure 4

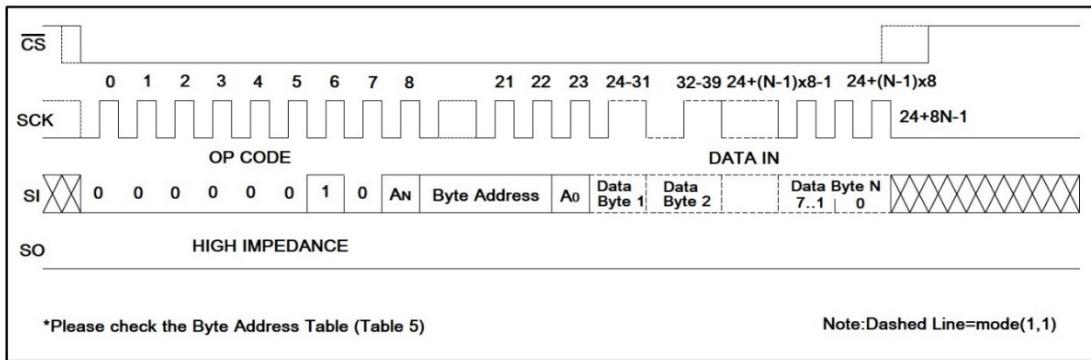
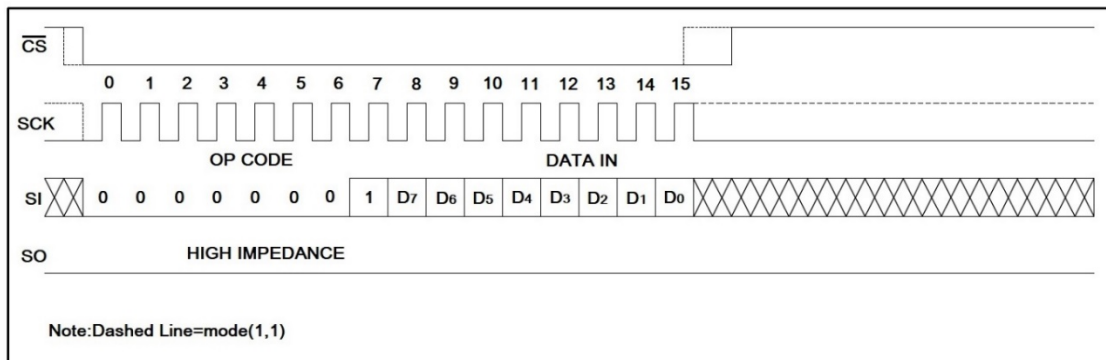


Table 5

Device	Address Significant Bits	Address Don't Care Bits	Address Clock Pulses
Main Memory Array	A12 – A0	A15 – A13	16

**Write Status Register:** The Status Register is written by sending a WRSR instruction according to timing shown in Figure 5. Only bits 2, 3, 4, 5, 6 and 7 can be written using the WRSR command.

Figure 5

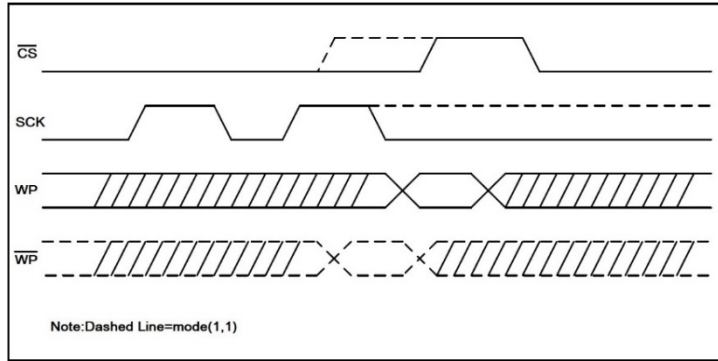


**Write Protection:** The Write Protect ( $\overline{WP}$ ) pin can be used to protect the Block Protect bits BP0 and BP1 against being inadvertently altered. When ( $\overline{WP}$ ) is low and the SRWD bit is set to “1”, write operations to the Status Register are inhibited. ( $\overline{WP}$ ) going low while ( $\overline{CS}$ ) is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, ( $\overline{WP}$ ) going low will have no effect on any write operation to the



Status Register. The ( $\overline{WP}$ ) pin function is blocked when the SRWD bit is set to “0”. The ( $\overline{WP}$ ) input timing is shown in Figure 6.

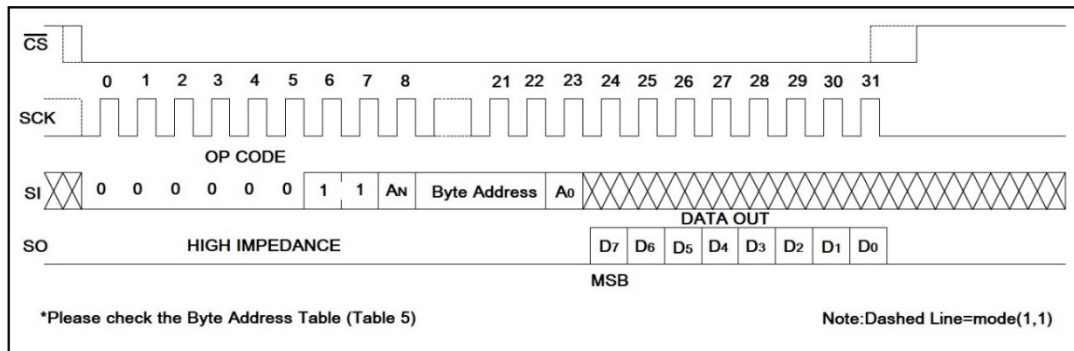
Figure 6



### 3. Read Operations

**Read from Memory Array:** To read from memory, the host sends a READ instruction followed by a 16-bit address. After receiving the last address bit, the A25C64 will respond by shifting out data on the SO pin (as shown in Figure 7). Sequentially stored data can be read out by simply continuing to run the clock. The internal address pointer is automatically incremented to the next higher address as data is shifted out. After reaching the highest memory address, the address counter “rolls over” to the lowest memory address, and the read cycle can be continued indefinitely. The read operation is terminated by taking  $\overline{CS}$  high.

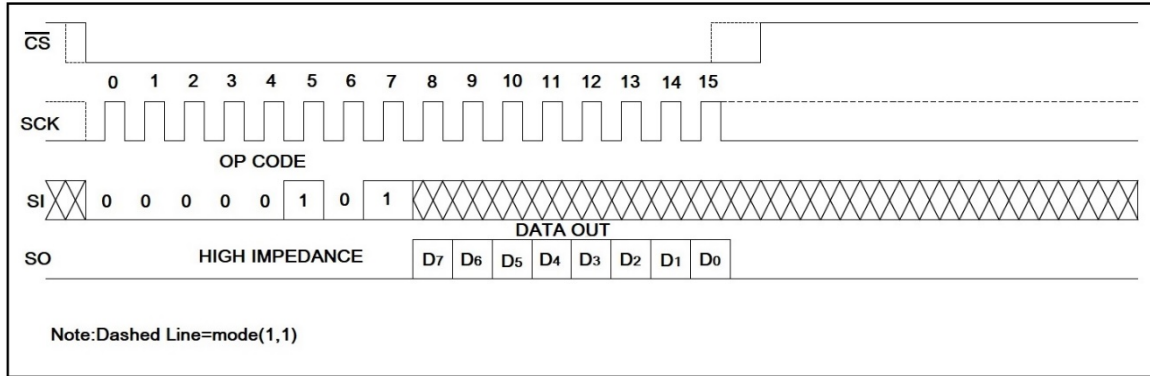
Figure 7



**Read Status Register:** To read the status register, the host simply sends a RDSR command. After receiving the last bit of the command, the A25C64 will shift out the contents of the status register on the SO pin (Figure 8). The status register may be read at any time, including during an internal write cycle.



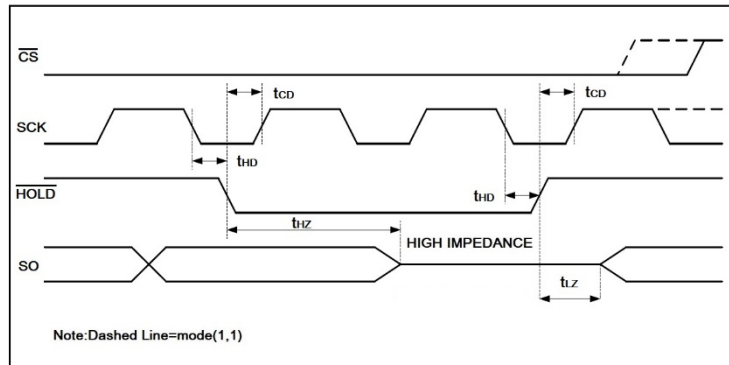
Figure 8



#### 4. Hold Operation

The  $\overline{\text{HOLD}}$  input can be used to pause communication between host and A25C64. To pause,  $\overline{\text{HOLD}}$  must be taken low while SCK is low (Figure 9). During the hold condition the device must remain selected ( $\overline{\text{CS}}$  low). During the pause, the data output pin (SO) is tri-stated (high impedance) and SI transitions are ignored. To resume communication,  $\overline{\text{HOLD}}$  must be taken high while SCK is low.

Figure 9



#### 5. Design Considerations

The A25C64 device incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device will power up into Standby mode after  $V_{CC}$  exceeds the POR trigger level and will power down into Reset mode when  $V_{CC}$  drops below the POR trigger level. This bi-directional POR behavior protects the device against 'brown-out' failure following a temporary loss of power.

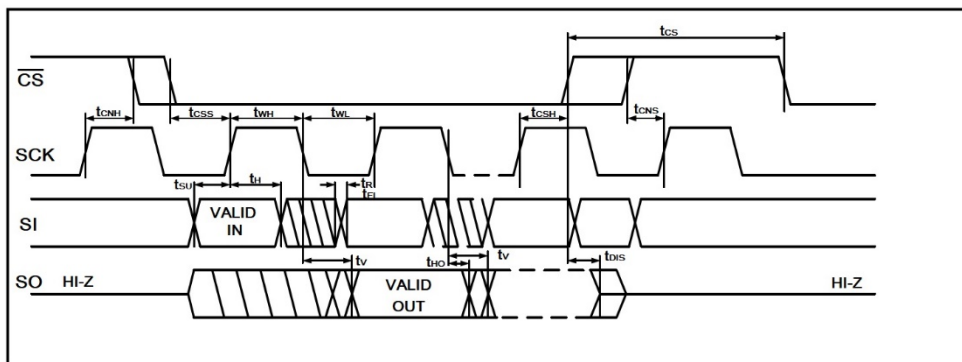
The A25C64 device powers up in a write disable state and in a low power standby mode. A WREN instruction must be issued prior to any writes to the device.



After power up, the  $\overline{CS}$  pin must be brought low to enter a ready state and receive an instruction. After a successful byte/page write or status register write, the device goes into a write disable mode. The  $\overline{CS}$  input must be set high after the proper number of clock cycles to start the internal write cycle. Access to the memory array during an internal write cycle is ignored and programming is continued. Any invalid op-code will be ignored and the serial output pin (SO) will remain in the high impedance state.

### BUS TIMING

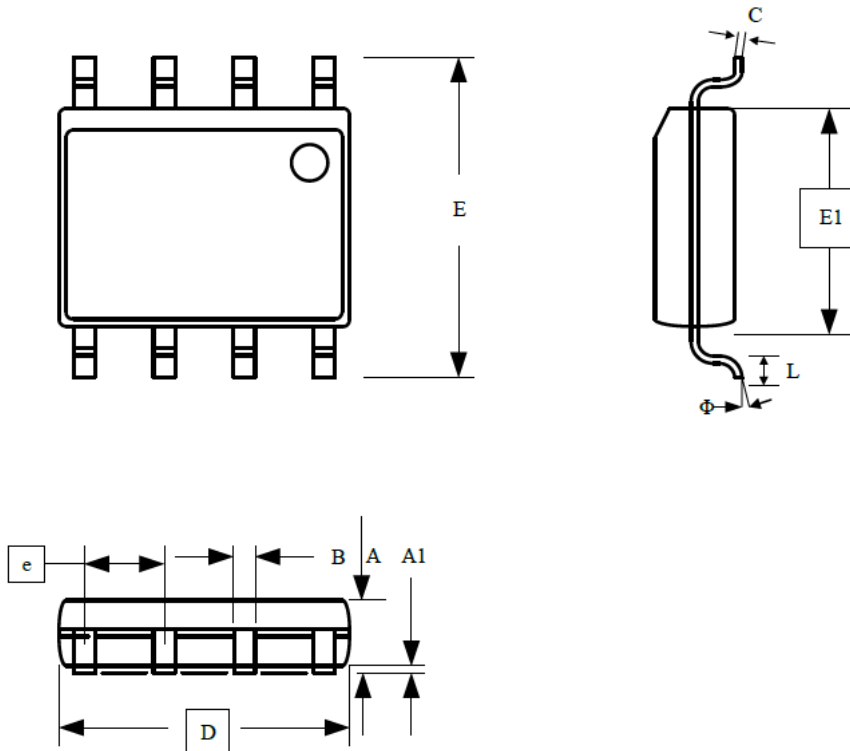
Figure 10





**PACKAGE INFORMATION**

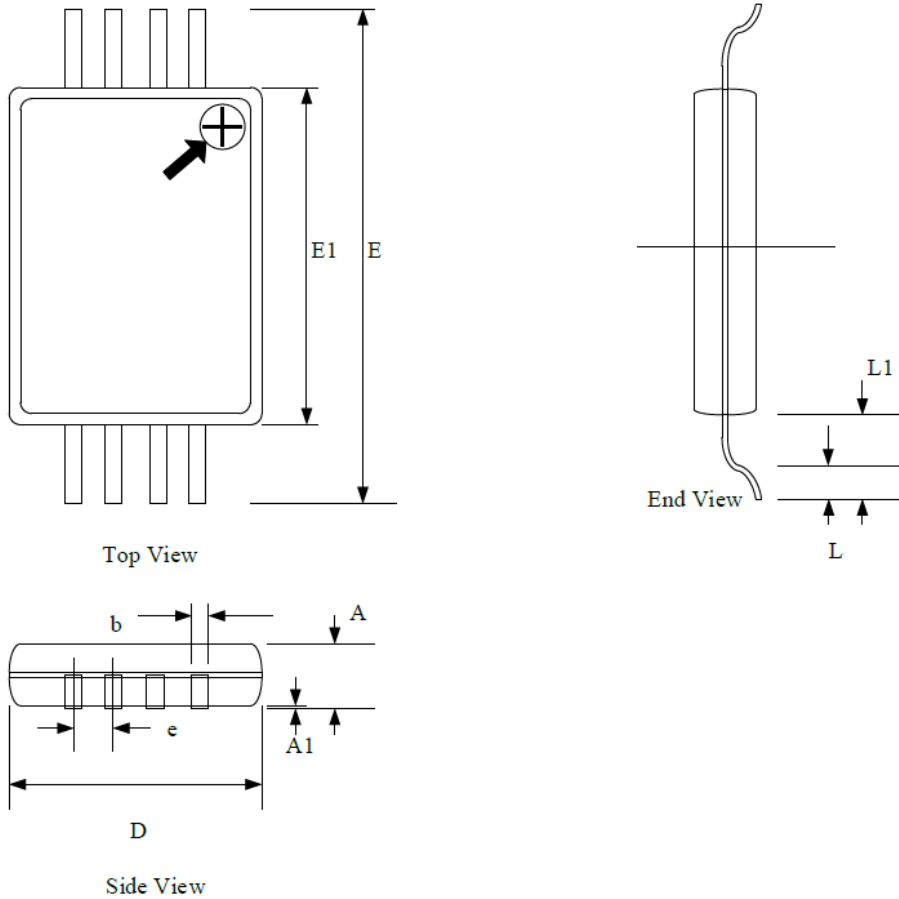
Dimension in SOP8 (Unit: mm)



Symbol	Min	Max
A	1.350	1.750
A1	0.100	0.230
B	0.390	0.480
C	0.210	0.260
D	4.700	5.100
E1	3.700	4.100
E	5.800	6.200
e	1.270 BSC	
L	0.500	0.800
$\theta$	0°	8°



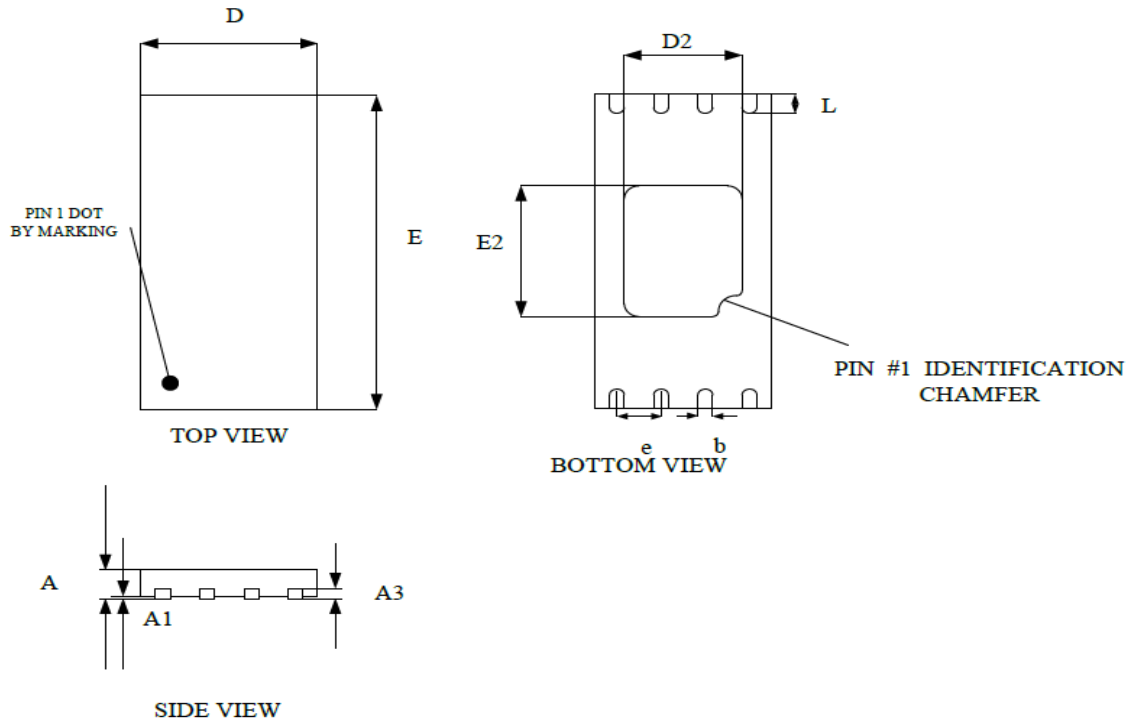
Dimension in TSSOP8 Package (Unit: mm)



Symbol	Min	Max
D	2.900	3.100
E	6.200	6.600
E1	4.300	4.500
A	-	1.200
A1	0.050	0.150
b	0.210	0.300
e	0.650 BSC	
L	0.450	0.750
L1	1.000 REF	



Dimension in DFN8 (Unit: mm)



Symbol	Min	Max
A	0.500	0.600
A1	0.000	0.050
A3	0.152 REF	
D	1.900	2.100
E	2.900	3.100
b	0.200	0.300
L	0.250	0.350
D2	1.300	1.500
E2	1.200	1.400
e	0.500 BSC	





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