DESCRIPTION

The AP8344 provides the necessary features to implement AC-DC or DC-to-DC fixed frequency current-mode control schemes with a minimum number of external components.

Protection circuitry includes undervoltage lockout (UVL) and current limiting. Internally implemented circuits include under-voltage lockout featuring start up current less than 0.5mA, a precision reference trimmed for accuracy at the error amp input, logic to ensure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N channel MOSFETs, is low in the off state.

The AP8344 is available in DIP8 and SOP8 Packages.

FEATURES

- Optimized for Off-Line and DC to DC Converts
- Low Start Up Current(<0.5mA)
- Automatic Feed Forward Compensation
- Pulse-by-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout with Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500kHz Operation
- Low Ro Error Amp

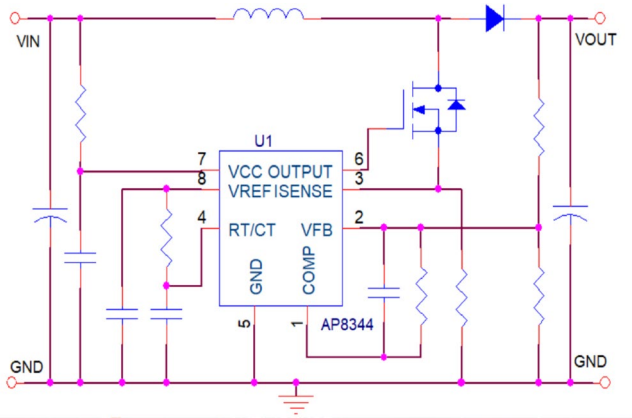
APPLICATION

- Switching regulators of any polarity
- Transformer-coupled DC-DC converters

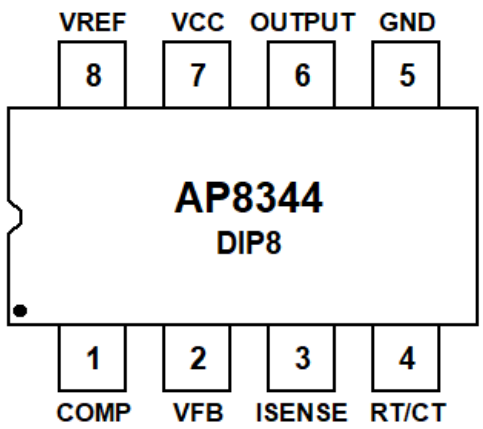
ORDERING INFORMATION

Package Type	Part Number	
DIP8 SPQ: 50pcs/Tube	P8	AP8344P8U
		AP8344P8VU
SOP8 SPQ: 4,000pcs/Reel	M8	AP8344M8R
		AP8344M8VR
Note	R: Tape & Reel U: Tape & Tube V: Halogen free Package	
AiT provides all RoHS products		

TYPICAL APPLICATION

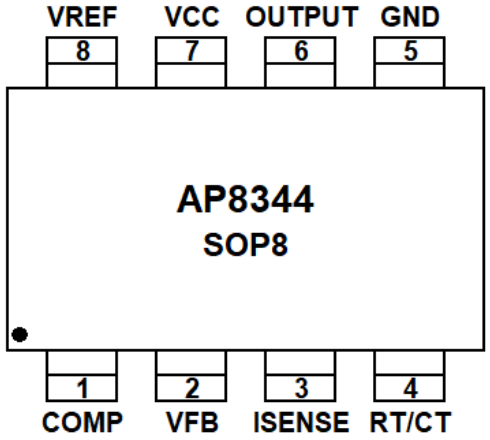


PIN DESCIPTION



DIP8, P8

Top View



SOP8, M8

Top View

#Pin		Symbol	Type	Function
DIP8	SOP8			
1	1	COMP	O	Error amplifier output, this pin is made available for loop compensation.
2	2	VFB	I	Voltage Feedback, the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	3	ISENSE	I	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	4	RT/CT	I/O	The Oscillator frequency and maximum output duty cycle are programmed by connecting resistor RT to Vref and capacitor CT to ground. Operation to 1 MHz is possible.
5	5	GND	G	Power ground.
6	6	OUTPUT	O	This output directly drives the gate of a power MOSFET. Peak currents up to 1A are sourced and sunk by this pin. The output switches at one-half the oscillator frequency.
7	7	VCC	I	Positive Supply
8	8	VREF	O	Reference output, provides charging current for capacitor CT though resistor RT.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

V_{CC}, Supply Voltage	Low Impedance Source	30V
	I_{CC}<30mA	Self-Limiting V
I_O, Output Current		±1A
Output Energy (Capacitive Load)		5μJ
$V_{I(ANA)}$, Analog Inputs (Pin 2,3)		-0.3V ~ +6.30V
$I_{SINK(EA)}$, Error Amplifier Output Sink Current		10mA
P_D, Power Dissipation at T_{amb}≤25℃	DIP8	1W
	SOP8	0.75W
Tlead, Lead Temperature (10 Sec)		260℃
Tstg, Storage Temperature		-65℃ ~ +150℃
T_J, Junction Operating Temperature		+150℃

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

0≤T_A≤70≤C,V_{CC}=15V,R_T=10kΩ,C_T=3.3nF,unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
REFERENCE SECTION						
Output Voltage	V_{REF}	T_J=25℃, I_O=1mA	4.90	5	5.10	V
Line Regulation	$\triangle V_{REF}$	12≤V_{IN}≤25V	-	2	20	mV
Load Regulation	$\triangle V_{REF}$	1≤I_O=20mA	-	3	25	mV
Temperature Stability	-		-	0.20	-	mV/℃
Total Output Variation	-	Line, Load, Temp.	4.82	-	5.18	V
Total Output Variation	eN	10Hz≤f≤10kHz,Tj=25℃	-	50	-	μV
Long Term Stability	-	T_A=25℃,1000Hrs	-	5	25	mV
Output Short Circuit	I_{SC}	-	-30	-100	-180	mA
OSCILLATOR SECTION						
Initial Accuracy	fosc	T_J=25℃	49	52	55	kHz
Voltage Stability	$\triangle f/\triangle V_{CC}$	12≤V_{CC}≤25V	-	0.20	1	%
Temp Stability	-	Tmin≤T_A≤Tmax	-	5	-	%
Amplitude	V_{OSC}	Vpin 4 peak to peak	-	1.60	-	V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
ERROR AMPLIFIER SECTION						
Input Voltage	$V_{I(EA)}$	Vpin 1=1.25V	2.42	2.50	2.58	V
Input Bias current	I_{BIAS}	-	-	-0.10	-2	μA
A_{VOL}	-	2≤Vo≤4V	60	90	-	dB
Unity Gain Bandwidth	-	T_J=25℃	0.70	1	-	MHz
PSRR	-	I2≤V_{CC}≤5V	60	70	-	dB
Output Sink Current	Isink	Vpin 2=2.7V, Vpin 1=1.1V	2	12	-	mA
Output Source Current	Isource	Vpin 2=2.3V, Vpin 1=5V	-0.50	-1	-	mA
Vout High	-	Vpin 2=2.3V, RL=15kΩ to GND	5	6.20	-	V
Vout Low	-	Vpin 2=2.7V, Vpin 1=1.1V	-	0.80	1.10	V
CURRENT SENSE SECTION						
Gain (1)(2)	G_V		2.85	3	3.15	V/V
Maximum Input Signal (1)	$V_{I(MAX)}$	Vpin 1=5V	0.90	1	1.11	V
SVR	-	12≤V_{CC}≤25V	-	70	-	dB
Input Bias Current	I_{BIAS}	-	-	-2	-10	μA
Delay to Output	-	Vpin 3=0 ~ 2V	-	150	300	ns
OUTPUT SECTION						
Output Low Level	V_{OL}	Isink=20mA	-	0.10	0.40	V
		Isink=200mA	-	1.60	2.20	V
Output High Level	V_{OH}	Isource=20mA	13	13.50	-	V
		Isource=200mA	12	13.50	-	V
Rise Time	t_R	T_J=25℃,CL=1nF	-	50	150	ns
Fall Time	t_F	T_J =25℃,CL=1nF	-	50	150	ns
UVLO Saturation	-	Vcc=5V, Isink=10mA	-	0.70	1.20	V
UNDER-VOLTAGE LOCKOUT OUTPUT SECTION						
Start Threshold	$V_{TH(ST)}$		14.50	16	17.50	V
Min. Operating Voltage After Turn On	$V_{OPR\ (min)}$		8.50	10	11.50	V
PWM SECTION						
Maximum duty Cycle	$D_{(MAX)}$		47	48	50	%
Minimum Duty Cycle	$D_{(MIN)}$		-	-	0	%
TOTAL STANDBY CURRENT						
Start-up Current	I_{ST}		-	0.30	0.50	mA
Operating Supply Current	$I_{CC\ (opr)}$	Vpin 2=Vpin 3=0V	-	12	17	mA
V_{CC} Zener Voltage	V_Z	I_{CC} =25mA	-	34	-	V

(1) Parameters measured at trip point of latch with Vpin 2=0.

(2) Gain defined as: A=ΔVpin 1/ΔVpin 3; 0 ≤Vpin 3≤ 0.8V

TYPICAL PERFORMANCE CHARACTERISTICS

Fig 1. Vref Temperature Drift

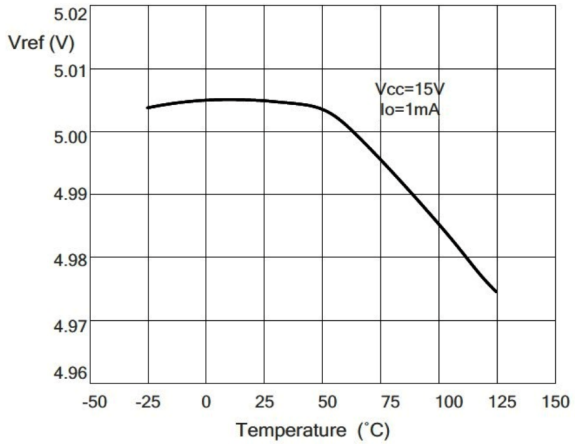


Fig 2. Istart Temperature Drift

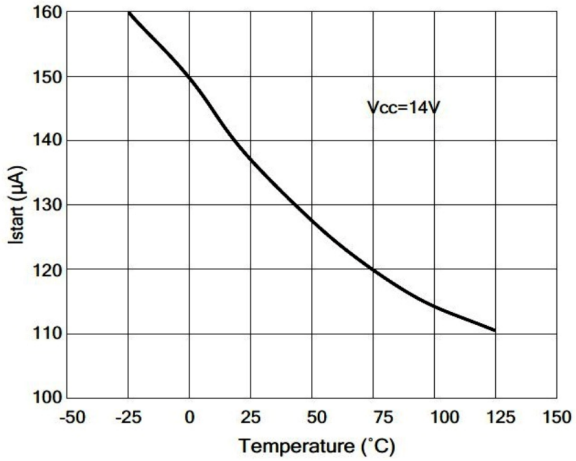


Fig 3. Icc Temperature Drift

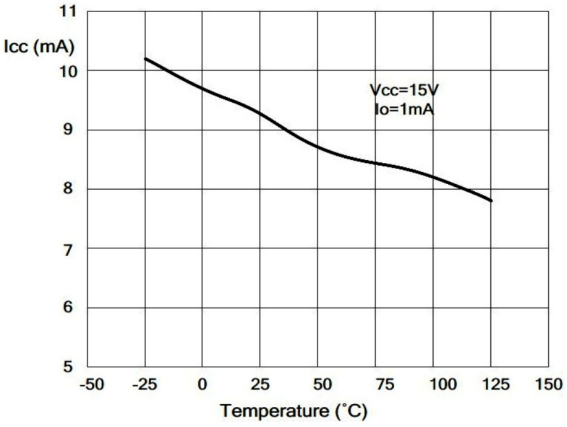


Fig 4. Output Saturation Characteristics

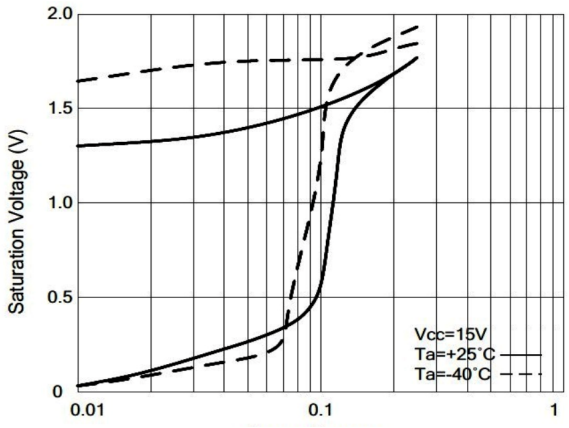
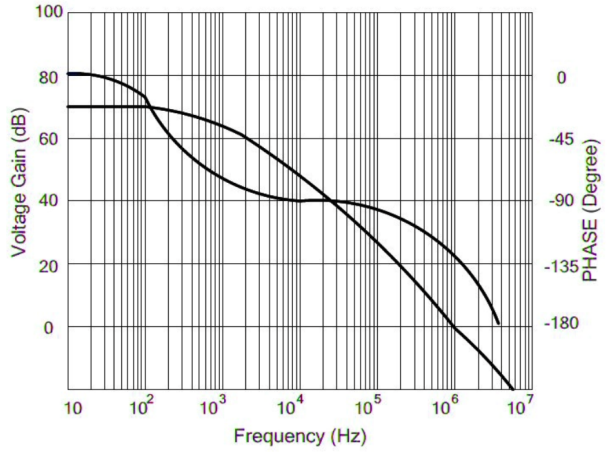
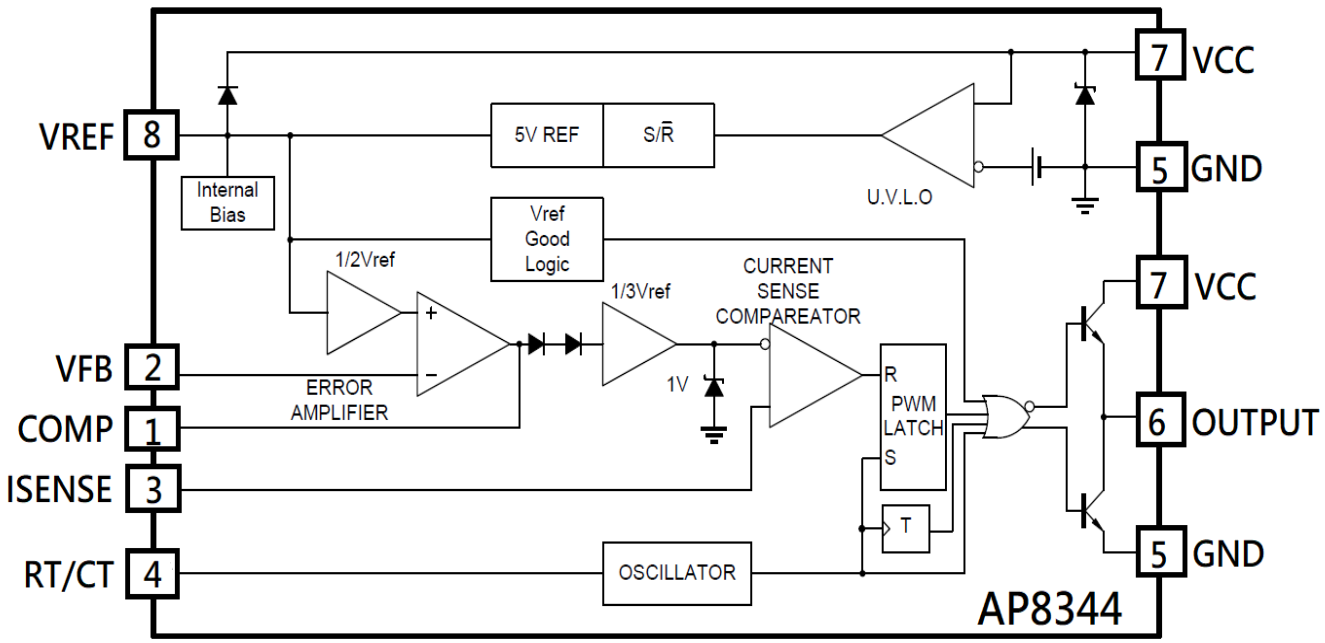


Fig 5. Error Amplifier Open-Loop Frequency Response

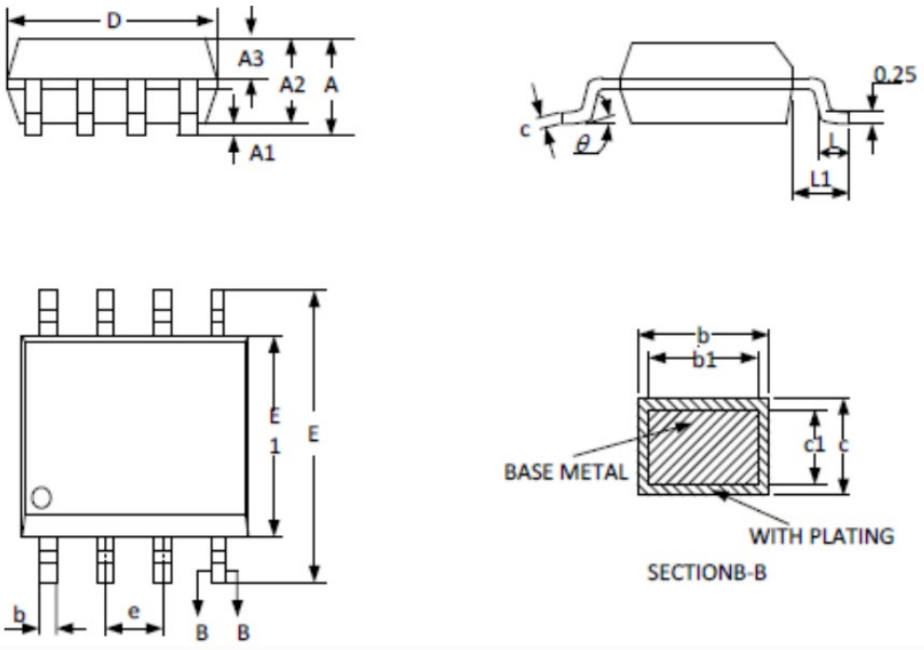


BLOCK DIAGRAM



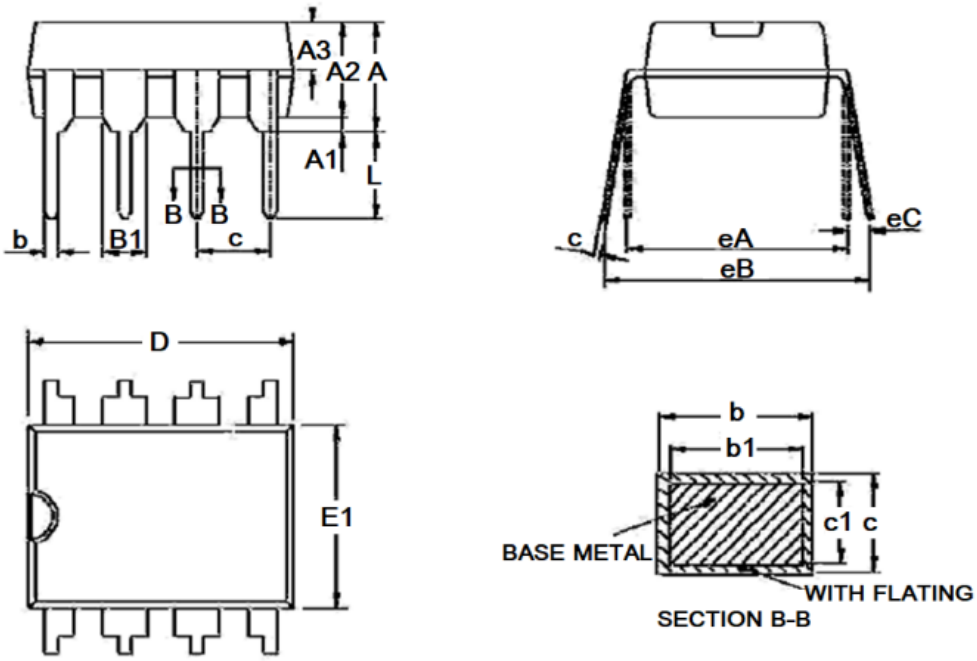
PACKAGE INFORMATION

Dimension in SOP8 (Unit: mm)



Symbol	Min.	Max.
A	-	1.770
A1	0.080	0.280
A2	1.200	1.600
A3	0.550	0.750
b	0.390	0.480
b1	0.380	0.430
c	0.210	0.260
c1	0.190	0.210
D	4.700	5.100
E	5.800	6.200
E1	3.700	4.100
e	1.270 BSC.	
L	0.500	0.800
L1	1.050 BSC.	
θ	0°	8°

Dimension in DIP8 (Unit: mm)



Symbol	Min.	Max.
A	3.600	4.000
A1	0.510	-
A2	3.000	3.400
A3	1.550	1.650
B1	1.520 BSC.	
b	0.440	0.530
b1	0.430	0.480
c	0.240	0.320
c1	0.230	0.270
D	9.050	9.450
E1	6.150	6.550
e	2.540 BSC.	
eA	7.620 BSC.	
eB	7.620	9.300
eC	0.000	0.840
L	3.000	-

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