



DESCRIPTION

The A7115D is a current mode monolithic buck switching regulator. Operating with an input range of 2.5V-7.2V, the A7115D delivers 1.5A of continuous output current with integrated P-Channel and N-Channel MOSFETs. The internal synchronous power switches provide high efficiency. At light loads, the regulator operates in low frequency to maintain high efficiency and low output ripples. Current mode control provides tight load transient response and cycle-by-cycle current limit.

The A7115D guarantees robustness with hiccup output short-circuit protection, FB short-circuit protection, start-up current run-away protection, input under voltage lockout protection, hot-plug in protection, and thermal protection.

The A7115D is available in SOT-25 and DFN8(2x2) Packages.

FEATURES

- 1.5MHz Switching Frequency
- Up to 1.5A Output Current
- Up to 95% Peak Efficiency
- 2.5V to 7.2V Operating Input Range
- Can Reach 100% Duty Cycle
- PWM Automatic/PFM Switching Duty Cycle Adjustable to Maintain a Large Load Range of High Efficiency, Low Ripple
- Short Circuit Protection

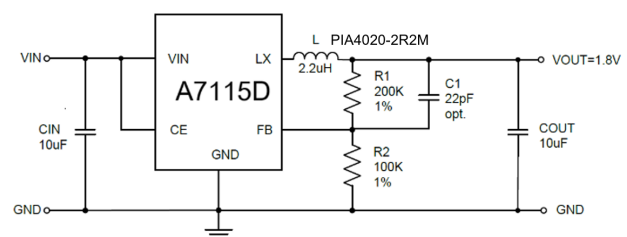
APPLICATION

- Set Top Boxes
- Telecom/Networking Systems
- Cameras, Video Equipment, Communications Equipment, Regulated Power Supply
- GPU/DDR Power Supply

ORDERING INFORMATION

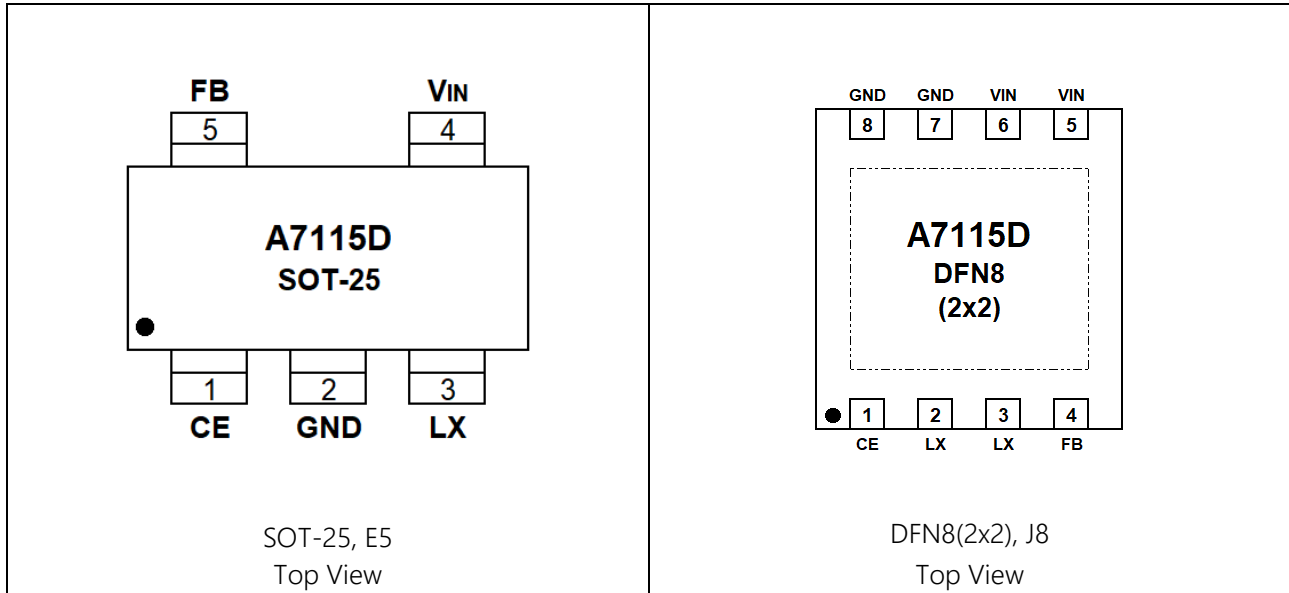
| Package Type | Part Number | |
|---------------------------------|---|------------|
| SOT-25 SPQ:3,000pcs/Reel | E5 | A7115DE5R |
| | | A7115DE5VR |
| DFN8(2x2) SPQ: 3,000pcs/Reel | J8 | A7115DJ8R |
| | | A7115DJ8VR |
| Note | V: Halogen free Package R: Tape & Reel | |
| AiT provides all RoHS products | | |

TYPICAL APPLICATION





PIN DESCRIPTION



| Pin # | | Symbol | Functions |
|--------|---------------|--------|---|
| SOT-25 | DFN8(2x2) | | |
| 1 | 1 | OUT | Drive EN Pin, High to Turn on the Regulator |
| 2 | 7, 8, Exposed | -IN | Ground |
| 3 | 2, 3 | NC | Internal Power Switch Output Port |
| 4 | 5, 6 | +IN | Power Input |
| 5 | 4 | V- | Output Feedback |

ABSOLUTE MAXIMUM RATINGS

| | | |
|-------------------------------------|-------------------------|-------|
| V_{IN} , Input Voltage | -0.3V ~ +7.50V | |
| V_{FB} , Output Voltage | -0.3V ~ +6.50V | |
| V_{LX} , Output Voltage | -0.3V ~ $V_{IN} + 0.3V$ | |
| V_{CE} , Voltage of the CE | -0.3V ~ $V_{IN} + 0.3V$ | |
| I_{LX} , LX Side Current | ±2A | |
| Pd, Power Dissipation | SOT-25 | 250mW |
| | DFN8(2x2) | 600mW |
| Topr, Operating Ambient Temperature | -40°C ~ +85°C | |
| Tstg, Storage Temperature | -55°C ~ +125°C | |

Stresses above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



ELECTRICAL CHARACTERISTICS

CIN=10uF, COUT=10uF, L=2.2uH, Ta = 25°C, unless otherwise noted.

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|---|-----------------------|-------|-------|-------|-------|
| Input Voltage | V _{IN} | - | 2.50 | - | 7.20 | V |
| VIN Under Voltage Lockout Threshold | UVLO | - | - | 2.40 | - | V |
| VIN Under Voltage Lockout Threshold Delay | UVLO_HYS | - | - | 500 | - | mV |
| OVP | OVP | - | - | 7.20 | - | V |
| OVP Delay | OVP_HYS | - | - | 250 | - | mV |
| Regulated Feedback Voltage | VFB | T _a = 25°C | 0.588 | 0.60 | 0.612 | V |
| Standby Current | ISTB | VCE=0V, VIN=5V | 0 | - | 1 | uA |
| Quiescent Current (PFM) | IQ | VFB=110%, ILOAD=0 | - | 40 | - | uA |
| Supply Current | I _{ACT} | VIN=5V | - | 280 | 500 | uA |
| Peak Current Limit | ILIM | VFB=90%, VIN=5V | 1.70 | - | - | A |
| Load Regulation | ΔV _{OUT} | ILOAD=10mA to 1.0A | - | 0.50 | - | % |
| Line Regulations | $\frac{\Delta V_{OUT}}{\Delta V_{IN} \times V_{OUT}}$ | VIN=2.5V to 6V | - | 0.04 | 0.40 | % |
| PFM Switch Point | ILOAD | VIN=3.6V, VOUT=1.8V | - | 30 | - | mA |
| Switch Frequency | FOSC | VOUT=100% | - | 1.50 | - | MHz |
| Maximum Duty Cycle | D _{MAX} | - | 100 | - | - | % |
| PFET On Resistance | PDSON_P | ISW=100mA | - | 0.30 | - | Ω |
| NFET On Resistance | PDSON_N | ISW=100mA | - | 0.20 | - | Ω |
| SW Side Leakage Current | PDSON_SW | VCE=0V, VIN=5V | - | ±0.01 | ±1 | uA |
| CE "High" Voltage | VCEH | VIN=5V | 1.20 | - | - | V |
| CE "Low" Voltage | VCEL | VIN=5V | - | - | 0.70 | V |
| Output Short | I _{OS} | FB<0.2V | - | 0.20 | - | A |
| Thermal Shutdown | TSHD | - | - | 160 | - | °C |
| Thermal Shutdown Delay | T_HYS | - | - | 25 | - | °C |



TYPICAL PERFORMANCE CHARACTERISTICS

Fig 1. Steady State Test

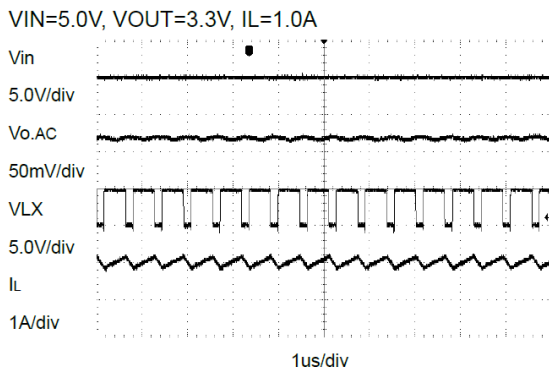


Fig 2. CE Open

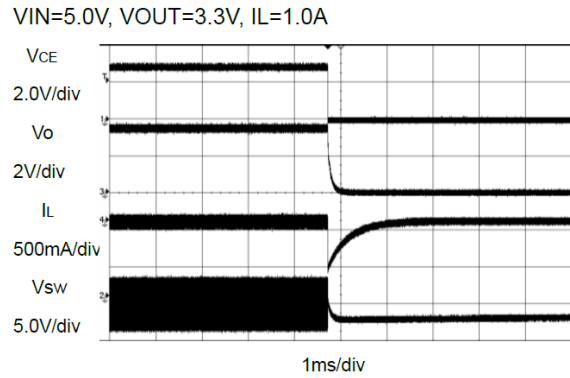


Fig 3. CE Shut Off

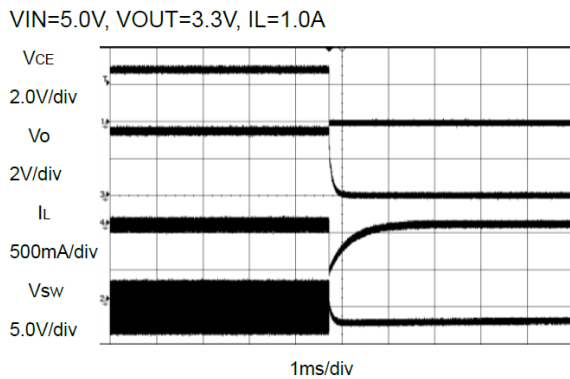


Fig 4. Light Load Operation

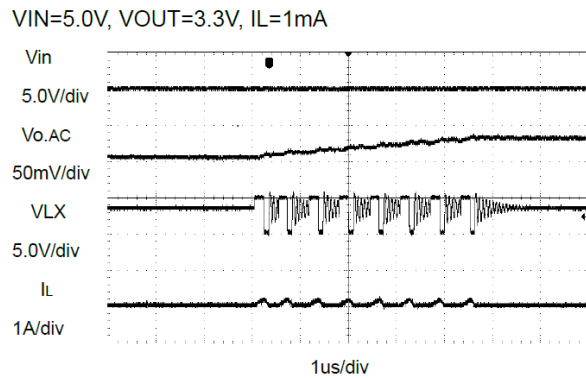


Fig 5. Medium Load Operation

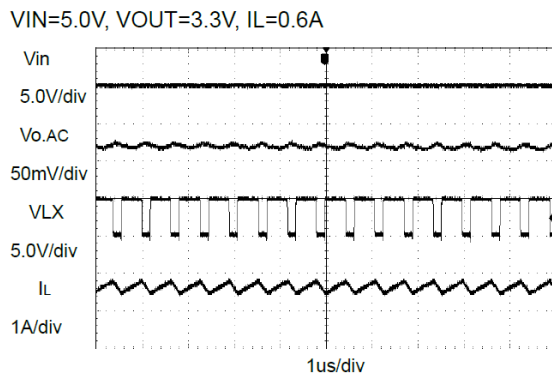


Fig 6. Heavy Load Operation

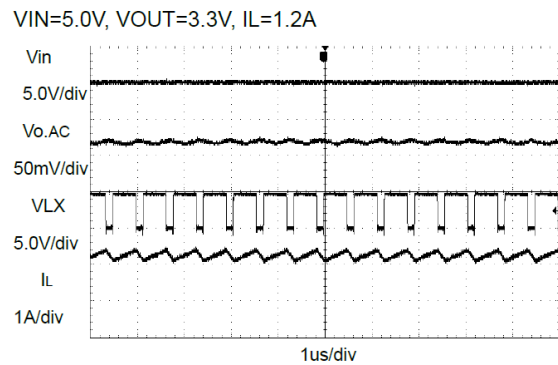




Fig 7. Quiescent Current vs. Temperature

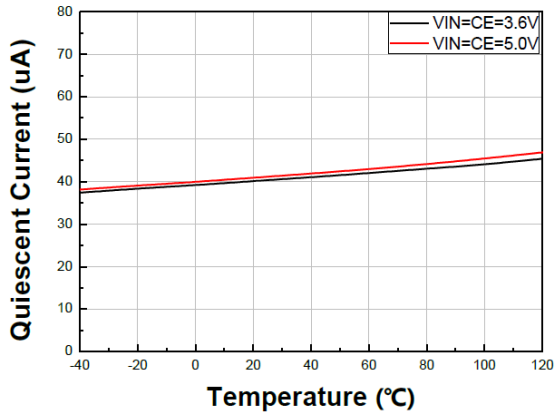


Fig 8. Frequency vs. Temperature

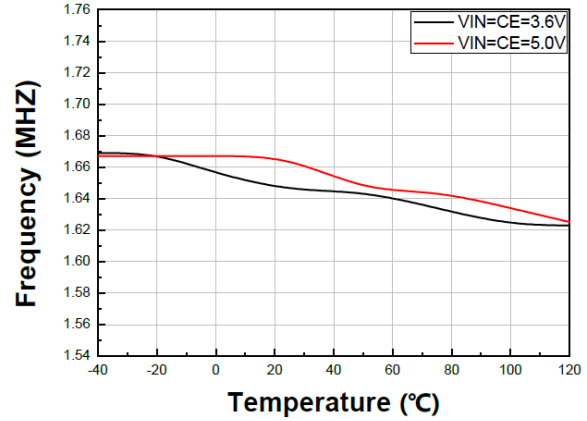


Fig 9. Output Voltage vs. Temperature

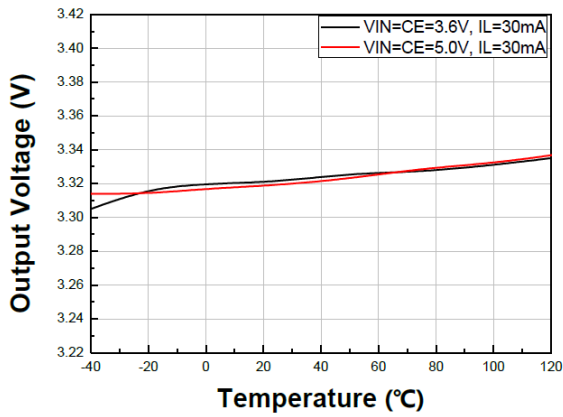


Fig 10. Reverse Output Current vs. Temperature

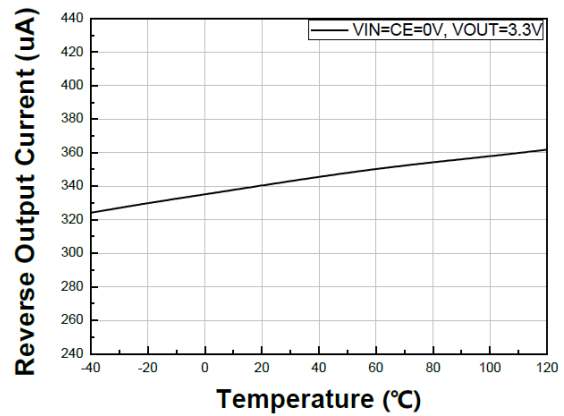


Fig 11. Efficiency vs. Temperature

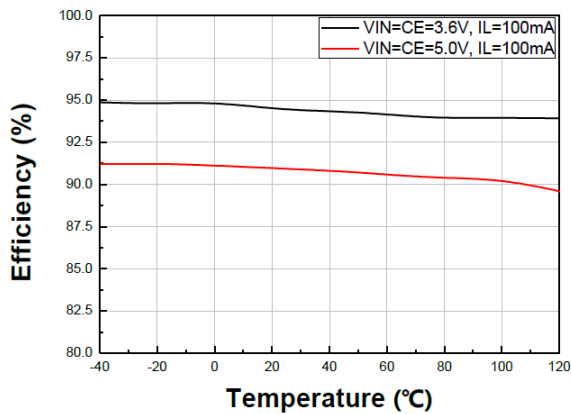


Fig 12. Efficiency @ VOUT=3.3V

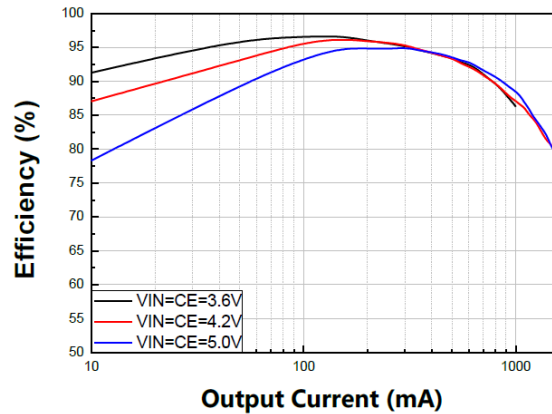




Fig 13. Efficiency @ VOUT=1.8V

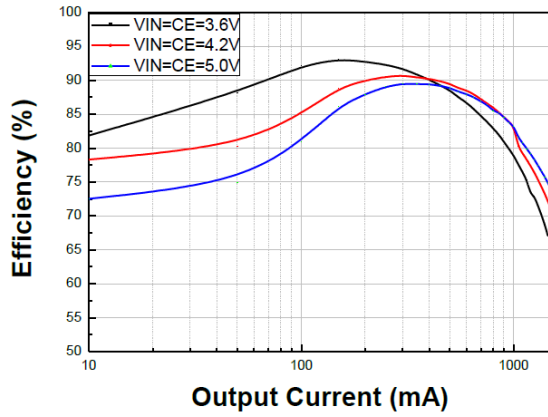


Fig 14. Efficiency @ VOUT=1.2V

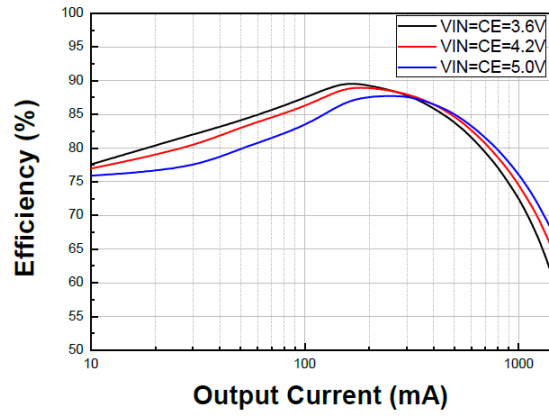


Fig 15. Quiescent Current vs. Input Voltage

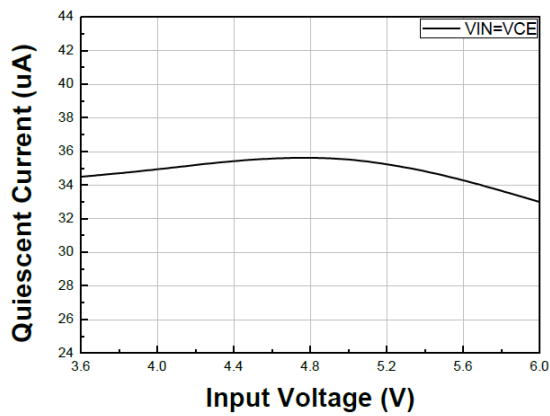
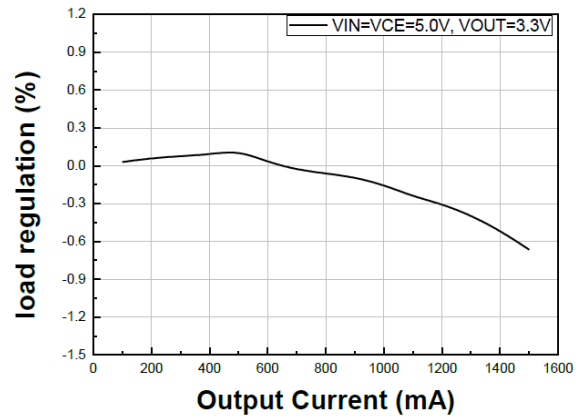
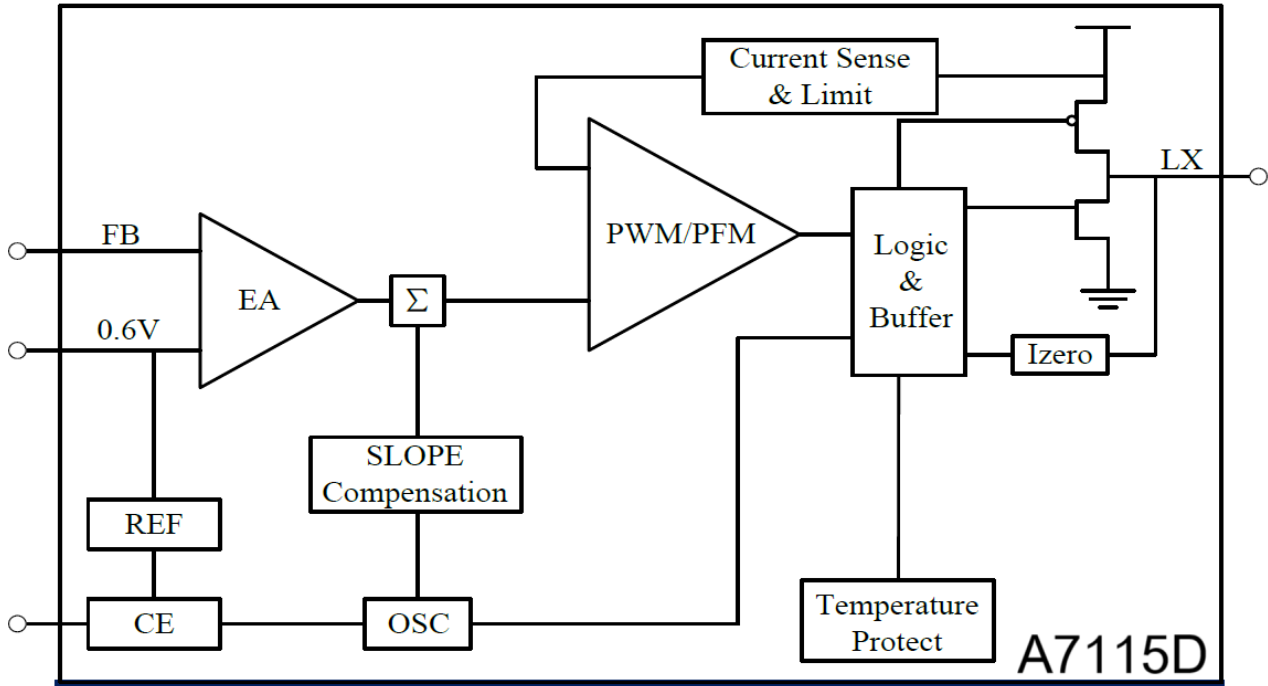


Fig 16. Load Regulation @ VOUT=3.3V





BLOCK DIAGRAM





DETAILED INFORMATION

Overview

The A7115D is a synchronous, current-mode step-down regulator. It regulates input voltages from 2.5V~7.2V down to an output voltage as low as 0.6V, and is capable of supplying up to 2A of load current.

The A7115D uses a constant frequency, current mode step-down architecture. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the current comparator, ICOMP, resets the RS latch. The peak inductor current at which ICOMP resets the RS latch, is controlled by the output of error amplifier EA.

When the load current increases, it causes a slight decrease in the feedback voltage, FB, relative to the 0.6V reference, which in turn, causes the EA amplifier's output voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator IRCMP, or the beginning of the next clock cycle.

PFM Mode

These A7115D operates in PFM mode at light load. In PFM mode, switch frequency is continuously controlled in proportion to the load current, i.e. switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples

Shut-Down Mode

The A7115D operates in shut-down mode when voltage at CE pin is driven below 0.7V. In shut-down mode, the entire regulator is off and the supply current consumed by the A7115D drops below 1uA.

Hot-Plug In Protection

If the VIN voltage exceeds 7.2V, IC will turn off power switch, entering over-voltage protection. It will remain in this state until VIN voltage is less than 6.9V.

Short Circuit Protection

When output is shorted to ground, the switching frequency is reduced to prevent the inductor current from increasing beyond PFET current limit.



Thermal Protection

When the temperature of the A7115D rises above 160°C, it is forced into thermal shut-down.

Only when core temperature drops below 135°C can the regulator becomes active again.

Typical Information

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage can be calculated by:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R1}{R2}\right) \quad \text{The recommended value of R2 is K}\Omega.$$

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{LOAD}}{f_s \times \Delta V_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where f_s is the switching frequency, ΔV_{IN} is the input ripple current.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 10uF ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(RESR + \frac{1}{8 \times f_s \times C_{OUT}}\right)$$

where C_{OUT} is the output capacitance value and RESR is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 10uF ceramic capacitor is recommended in typical application.



Inductor

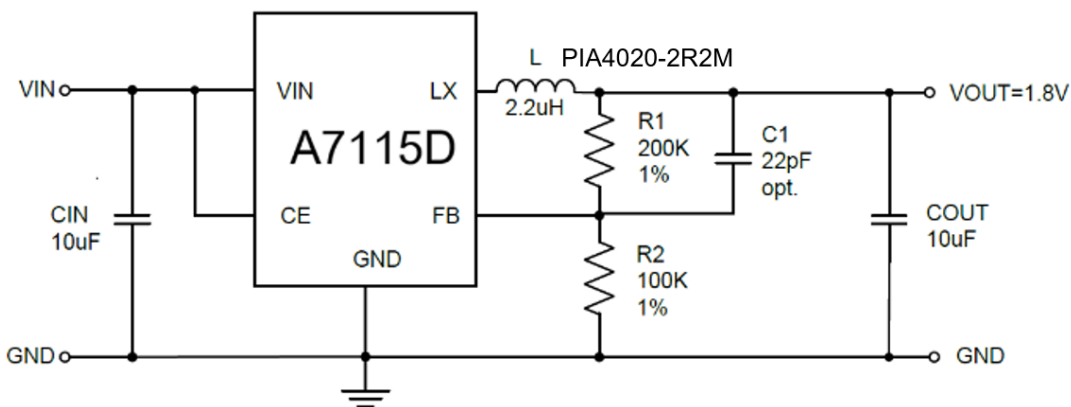
The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_s is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

AiT SEMi PIA4020-2R2M, 2.2uH inductor is recommended in typical application.

Reference Design



PCB Layout Note

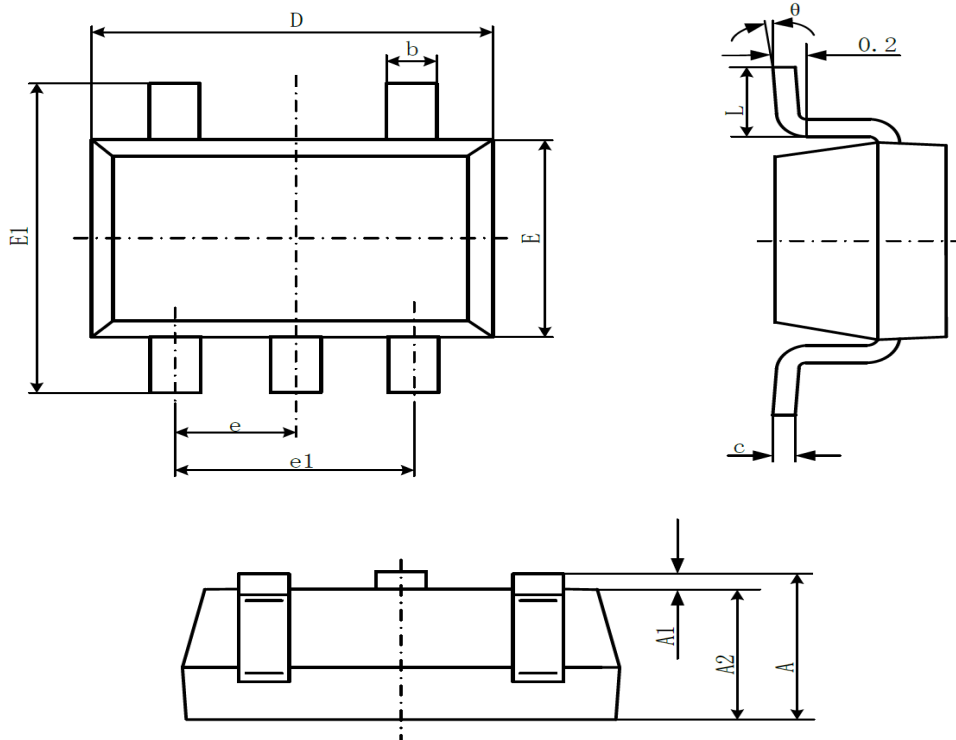
For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to A7115D (VIN pin and PGND) as possible to eliminate noise at the input pin.
2. The loop area formed by input capacitor and GND must be minimized.
3. Put the feedback trace as far away from the inductor and noisy power traces as possible.
4. The ground plane on the PCB should be as large as possible for better heat dissipation.



PACKAGE INFORMATION

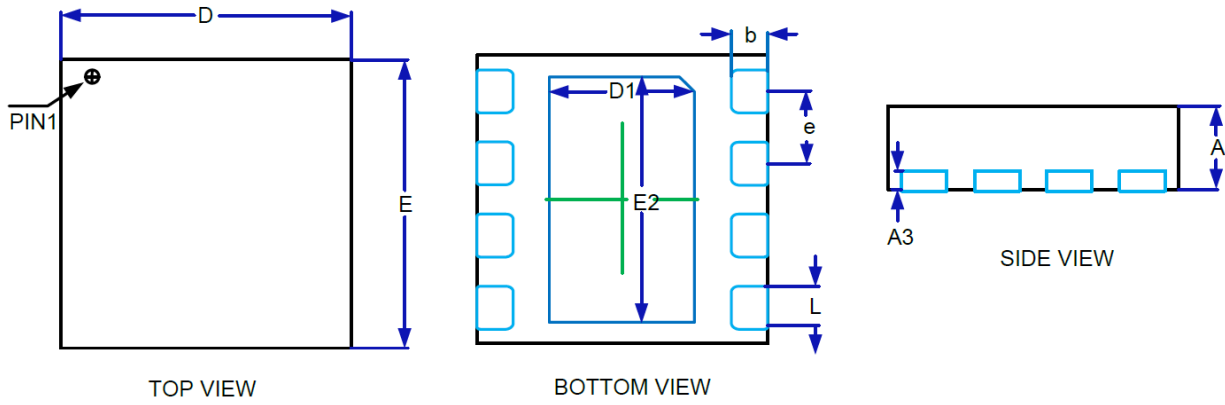
Dimension in SOT-25 (Unit: mm)



| Symbol | Millimeters | |
|--------|-------------|-------|
| | Min | Max |
| A | 1.050 | 1.250 |
| A1 | 0.000 | 0.100 |
| A2 | 1.050 | 1.150 |
| b | 0.300 | 0.500 |
| c | 0.100 | 0.200 |
| D | 2.820 | 3.020 |
| E | 1.500 | 1.700 |
| E1 | 2.650 | 2.950 |
| e | 0.950 BSC | |
| e1 | 1.800 | 2.000 |
| L | 0.300 | 0.600 |
| θ | 0° | 8° |



Dimension in DFN8(2x2) (Unit: mm)



| Symbol | Millimeters | |
|--------|-------------|-------|
| | Min | Max |
| A | 0.527 | 0.577 |
| A3 | 0.127 REF. | |
| b | 0.200 | 0.300 |
| D | 1.900 | 2.100 |
| D2 | 0.900 | 1.100 |
| E | 1.900 | 2.100 |
| E2 | 1.600 | 1.800 |
| e | 0.500 TYP. | |
| L | 0.250 | 0.350 |



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