DESCRIPTION

The A7106H employs constant on-time (COT) control architecture, providing excellent transient response. This high-voltage, step-down switching regulator can deliver up to 0.6 Amps of continuous current to the load and features an integrated high/ Low-side, high-voltage power MOSFET with a typical current limit of 0.8 Amps. It operates within a broad input voltage range of 5V to 100V and has built-in soft-start functionality. The A7106H is ideal for various step-down applications, particularly in the automotive, industrial, Motor Driver, and Telecom. Additionally, the device includes patented standby circuits that enable a quick transition from standby mode, reducing the need for external components.

The switching frequency can go as high as 1MHz, enabling the use of smaller components. Furthermore, features like thermal shutdown (OTP) and short-circuit protection (OCP) ensure reliable hiccup mode operation to protect both the circuitry and the IC. With a shutdown current of only 7.5μA, the A7106H is ideal for power-saving applications in various systems. It also includes an Open-Drain Power Good (PGOOD) that indicates the power is ready for system sequence design.

The A7106H is available in PSOP8 Packages.

ORDERING INFORMATION

Package Type	Part Number	
PSOP8 SPQ: 4,000pcs/Reel	MP8	A7106HMP8VR
Note	R: Tape & Reel V: Halogen free Package	
AiT provides all RoHS products		

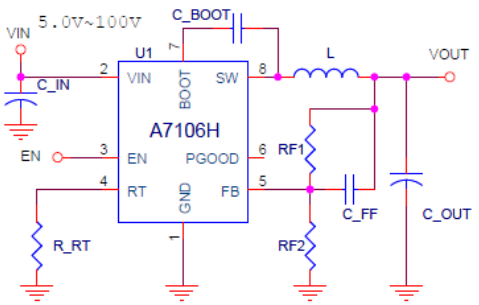
FEATURES

- Wide Input Voltage 5.0V–100V
- Up to 1 MHz switching frequency
- PWM Control for automotive, industrial, Motor Driver, and Telecom applications.
- Integrated 750mΩ High-Side and 300mΩ Low-Side MOSFET
- 65uA standby Current
- No Loop Compensation Components
- Integrated OD PGOOD indicator pin
- Precision ±1% Feedback reference.
- OCP, with OTP Thermal Shutdown
- PSOP8 Package with Thermal PAD

APPLICATION

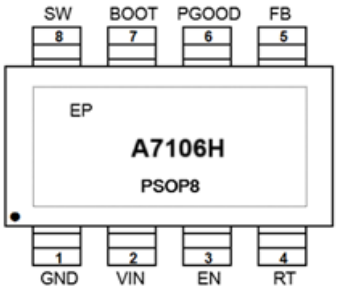
- Automotive and Industry Systems
- Motor Drives, and Telecom

TYPICAL APPLICATION DIAGRAM



L: 47uH: WSL05030-330M

PIN DESCRIPTION



PSOP8, MP8

Top View

PIN#	Symbol	Function
1	GND	Ground pin.
2	VIN	Input pin. Decouple this pin to GND with a low ESR ceramic capacitor.
3	EN	Enable Control pin. The device has an accurate 1.17V rising threshold and a programmable falling threshold. This pin can also be used for programming the VIN turn-on voltage with the resistor divider.
4	RT	On-time programming pin. A resistor between this pin and GND sets the buck switch on-time. $F_{SW}(kHZ) = \frac{3.2x\,Vout(V)}{RT(M\Omega)}$
5	FB	Output feedback pin. Connect this pin to the center point of the output resister divider to program the output voltage: V_{OUT} = 1.2x(1+R_{f1}/R_{f2})
6	PGOOD	Power good indicator pin. This pin is an open-drain output pin. Connect to a source voltage through a pull-up resistor.
7	BOOT	Boot-strap pin. Decouple this pin to the SW pin with a 10nF ceramic capacitor.
8	SW	Inductor pin. Connect to the switch node of the power inductor.
EP	Thermal PAD	Exposed pad of the package. Solder the EP the GND pin and connect to a large copper plane to reduce thermal resistance.

ABSOLUTE MAXIMUM RATINGS

VIN, EN, SW to GND	-0.3 ~ 110V
SW to GND (20ns pulse)	-3 ~ 110V
BS to GND	SW+6.6V
RT to GND	-0.3 ~ 6.6V
FB to GND	-0.3 ~ 6.6V
PGOOD to GND	-0.3 ~ 30V
P_D, Power Dissipation @T_A=25℃	3.3W
$\theta_{JA(Junction\ to\ ambient)}$, Package Thermal Resistance	30℃/W
$\theta_{JC(Junction\ to\ case)}$, Package Thermal Resistance	10℃/W
T_J, Operating Junction Temperature	-40 ~ 160℃
T_{stg}, Storage Temperature	-65 ~ 160℃
T_{SLD}, Soldering Temperature (10 second)	260℃

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN.	MAX.	Units
VIN Voltage	4.5	100	V
EN Voltage	-0.3	100	V
SW Voltage	-0.3	100	V
Operating Junction Temperature	-40	+125	℃

ESD RATINGS

		Value	Units
Electrostatic discharge V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDES JS-001, SW, BOOT, EN, RT, FB, PGOOD (1).	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, SW, BOOT, EN, RT, FB, PGOOD (2).	±500	V

(1) JEDEC document JEP155 states the 500V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states the 250V CDM allows safe manufacturing with a standard ESD control process

ELECTRICAL CHARACTERISTICS

V_{IN}=24V, V_{OUT}=5V, L=47μH, C_{OUT}=22μF, Typical values correspond to T_J=25℃, Minimum and Maximum limits apply over the full junction temperature range (-40℃ to 125℃) unless otherwise indicated.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
INPUT VOLTAGE						
Input Voltage	V_{IN}	-	5.0	-	100	V
SUPPLY CURRENT						
Shutdown Current	$I_{SHUTDOWN}$	V_{EN} = 0V	-	7.5	-	μA
Standby Current	$I_{STANDBY}$	V_{EN} = V_{IN} I_{OUT} = 0A	-	65	-	μA
FEEDBACK						
Feedback Reference Voltage	V_{REF}	-	1.182	1.2	1.218	V
EN/UVLO						
EN Rising Threshold	V_{ENH}	V_{IN} = 48V, I_{OUT} = 0.1A	1.0	1.17	1.24	V
Hysteresis Input Current	$I_{EN\_Hysteresis}$	V_{IN} = 48V, I_{OUT} = 0.1A	-1	-1.6	-2.2	μA
PGOOD						
FB Rising Threshold for PGOOD Low to High	V_{PGH}	V_{FB} rising	1.05	1.15	1.25	V
FB Falling Threshold for PGOOD High to Low	V_{PGL}	V_{FB} falling	0.95	1.05	1.15	V
FREQUENCY						
Programmable Switching Frequency Range	F_{SW}	$F(kHZ) = \frac{3.2x\ Vout(V)}{R_T(M\Omega)}$	100	-	1000	kHz
TIMMING						
Minimum on-time	t_{ON-MIN}	-	-	50	-	ns
Minimum off-time	$t_{OFF-MIN}$	-	-	270	-	ns
POWER MOSFET						
High-side MOSFET R_{DSON}	$R_{DSON-HS}$	Tested at T_J = 25℃	-	0.75	0.8	Ω
Low-side MOSFET R_{DSON}	$R_{DSON-LS}$	Tested at T_J = 25℃	-	0.3	0.35	Ω
CURRENT LIMITED PROTECTION						
High-side MOSFET Peak Current Limit	$I_{PEAK-HS}$	Only tested at T_J = 25℃	0.7	1	1.4	A
Low-side MOSFET Valley Current Limit	$I_{VALLEY-LS}$	Only tested at T_J = 25℃	0.5	0.6	0.7	A
SOF START						
Soft-start Time	t_{SS}	-	-	3	-	ms
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	T_{SD}	T_J rising	-	160	-	℃
Thermal Shutdown Hysteresis	T_{HYS}	-	-	25	-	℃

TYPICAL PERFORMANCE CHARACTERISTICS

Fig 1. Efficiency at 12Vout

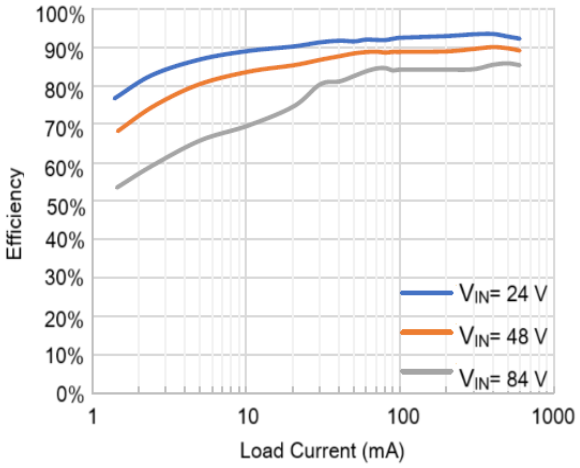


Fig 2. Load and Line Regulation

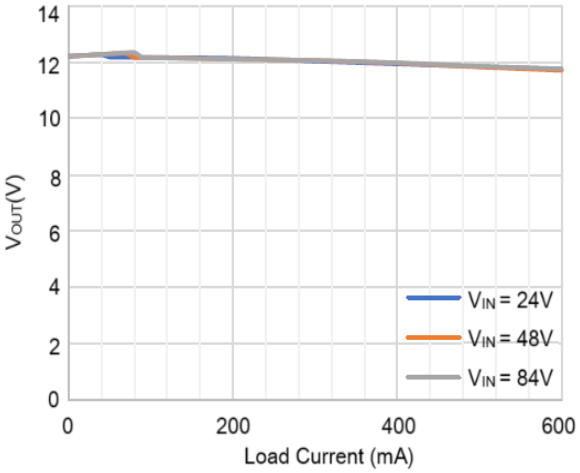


Fig 3. Startup from V_{IN}

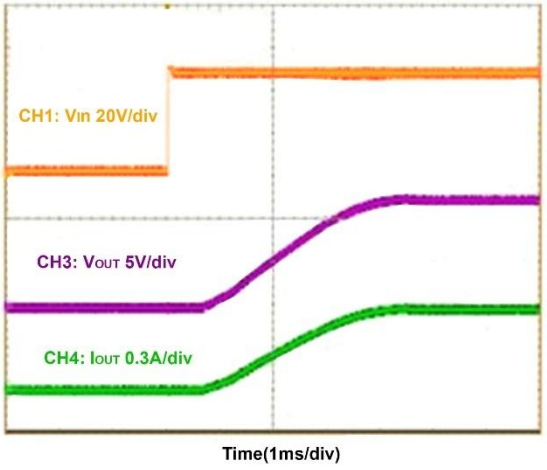


Fig 4. Shutdown from V_{IN}

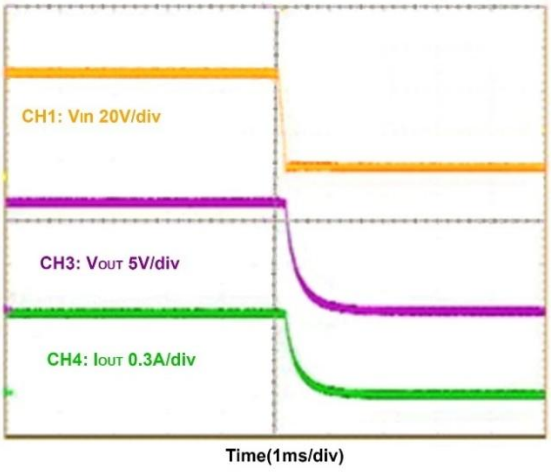


Fig 5. Startup from EN

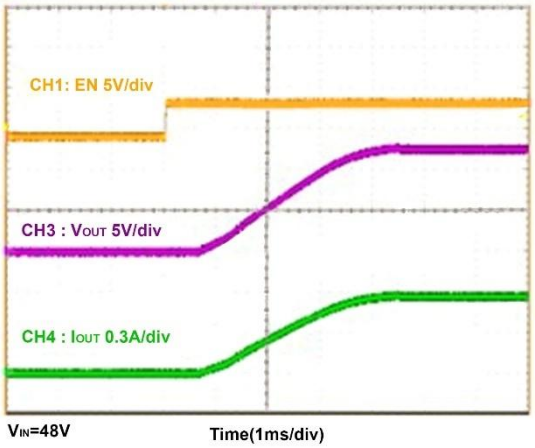


Fig 6. Shutdown from EN

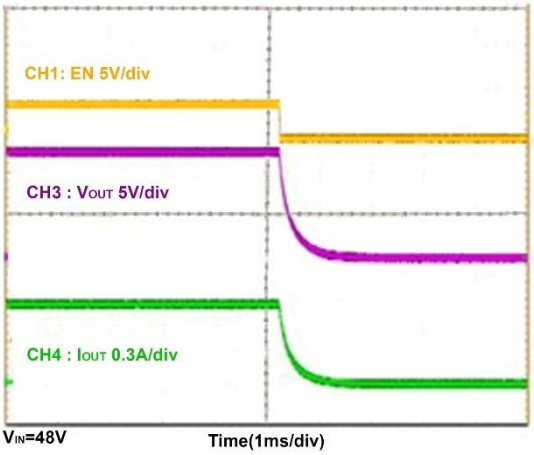


Fig 7. Short Protection and Recovery

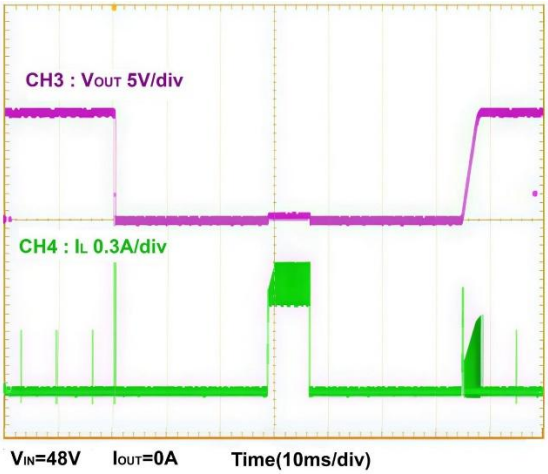


Fig 8. Short Protection and Recovery

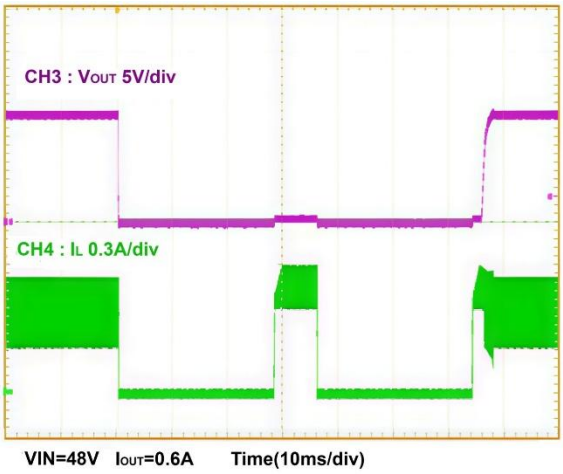


Fig 9. Load Transient

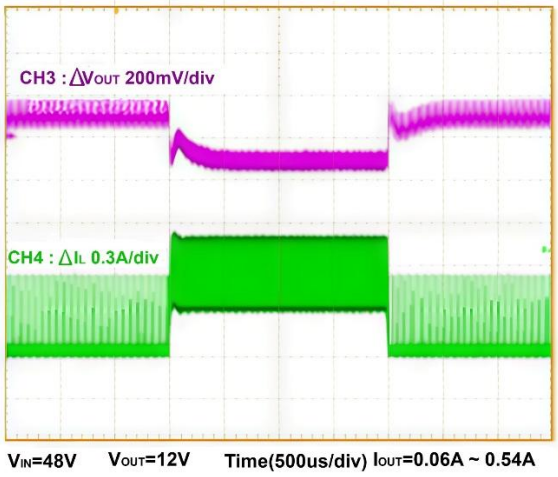


Fig 10. Load Transient

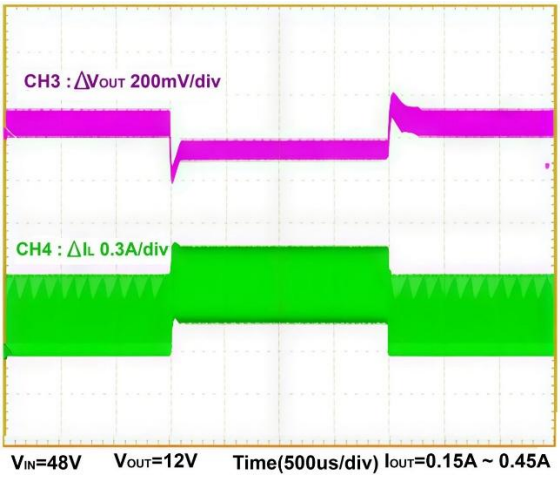


Fig 11. Out Ripple

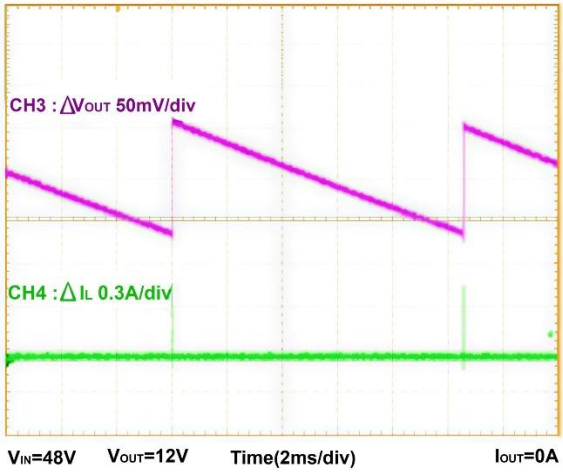
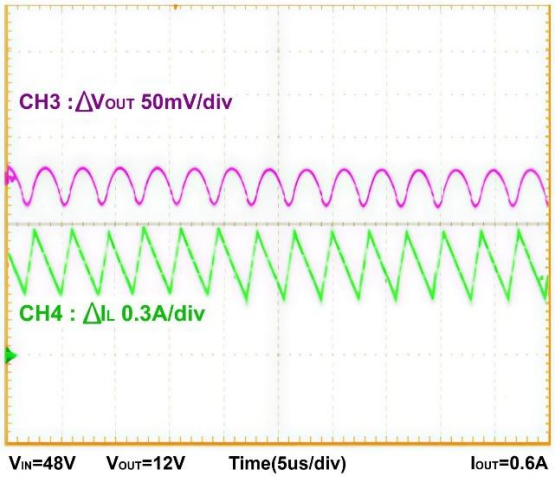
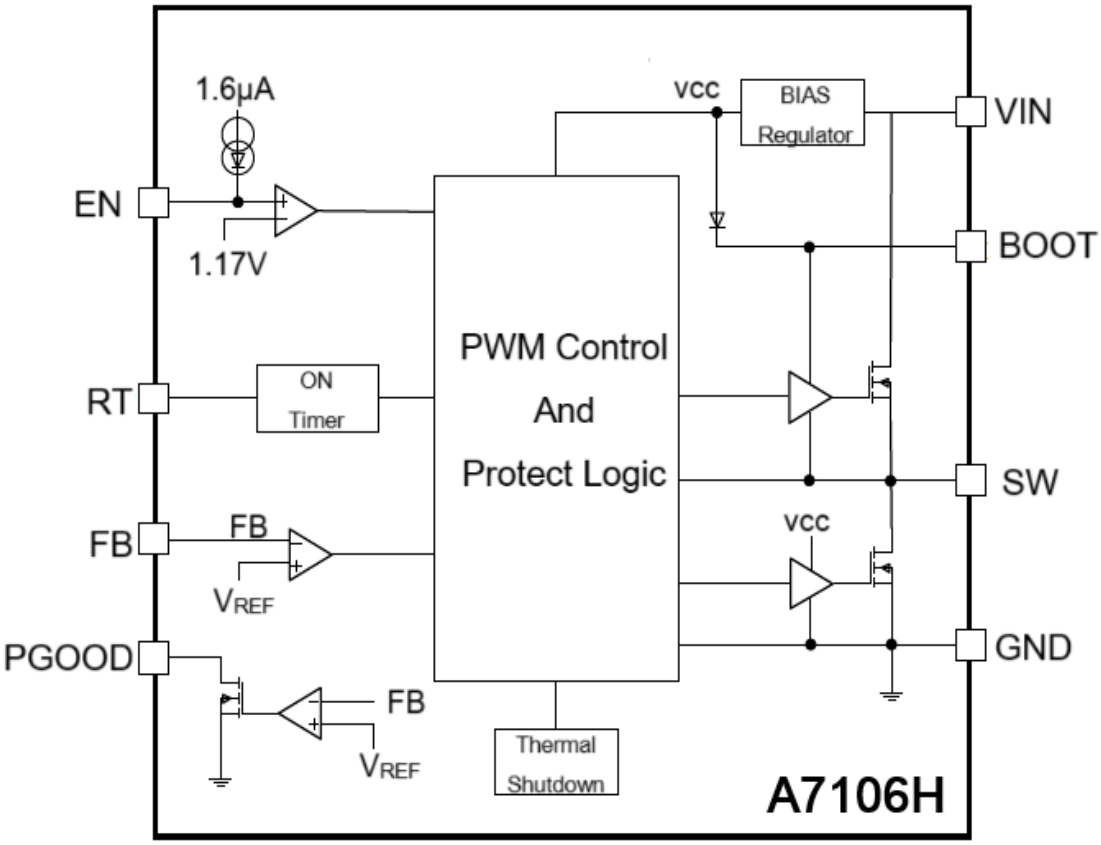


Fig 12. Out Ripple



BLOCK DIAGRAM



DETAILED INFORMATION

Operation Overview

The A7106H functions within a broad input voltage range of 5.0V to 100V. Featuring an integrated main MOSFET, it can provide an output current of up to 06A DC load current. The A7106H utilizes constant on-time (COT) control architecture, ensuring outstanding transient response. Control loop compensation is not required for this regulator, reducing design time and external component count. And the pin arrangement is designed for a simple layout requiring only a few external components.

Because of high integration in the A7106H, the application circuit is very simple. Only the on-timer resistor R_T, the feedback resistors (R_{f1} and R_{f2}), the BOOT capacitor C_{BOOT}, the feedforward capacitor C_{ff}, the input capacitor C_{IN}, the output capacitor C_{OUT}, and the output inductor L need to be selected for the targeted applications.

Switching Frequency (RT)

The switching frequency of the A7106H is determined by the on-time resistor on RT pin. As shown formula below, in 5V_{OUT} application 51kΩ resistor establishes a switching frequency of 320kHz. It's important to note that the final switching frequency is influenced not only by component tolerances but also by t_{ON-MIN} and $t_{OFF-MIN}$.

The formula is $F(\mathrm{kHZ}) = \frac{3.2\mathrm{x}\ \mathrm{Vout(V)}}{R_T(\mathrm{M\Omega})}$

Output Voltage Program

Choose R_{f1} and R_{f2} to program the output voltage. For target V_{OUT} setpoint, calculate R_{f1} and R_{f2} using below equation: (Better RF1/ FR2 is a 1% resistor)

$$V_{OUT} = 1.2V \times \left(1 + \frac{R_{f1}}{R_{f2}}\right)$$

For most applications, it is recommended to use a feedback resistor (R_{f1}) between 100kΩ and 500kΩ. Larger feedback resistors consume less DC power, which is important for maintaining efficiency at low loads. However, using excessively large resistors is not advisable, as they can increase the susceptibility of the feedback path. Additionally, incorporating a feedforward capacitor (C_{ff}) is highly recommended, as they can enhance system stability and improve transient responses. draw less DC, which is crucial for maintaining efficiency at light loads. However, excessively large resistors

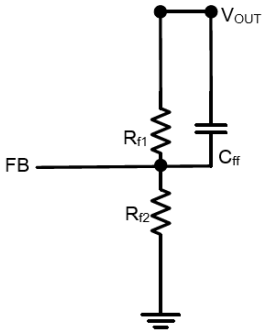


Fig.13 Feedback Resistance

are not recommended as they can reduce system stability and improve transient responses.

Input Capacitor (C_{IN})

An input capacitor is essential for reducing the input ripple voltage and supplying AC current to the buck converter during each switching cycle. The input ripple voltage, ΔVIN, across the input capacitor is calculated as follows:

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1-D)}{F_{sw} \times C_{IN}} + I_{OUT} \times R_{ESR}$$

The capacitance of input capacitor is calculated as:

$$C_{IN} \geqq \frac{I_{OUT} \times D \times (1-D)}{F_{sw} \times (\Delta V_{IN} - I_{OUT} \times R_{ESR})}$$

To reduce the potential noise issue, it is advisable to use a capacitor rated X5R or higher with an appropriate voltage rating. This capacitor should be positioned near the VIN and GND pins to minimize the loop area created by the C_{IN} and the V_{IN}/GND connections. For this application, a 1μF low ESR ceramic capacitor is recommended.

Output Inductor (L)

It is recommended to choose the ripple current of the inductor between 30% to 50% of the rated load current I_{OUT}(max) for most applications. The inductance is calculated as:

$$L = \frac{V_{OUT}}{F_{sw} \times \Delta V_{IL}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

And the peak current of inductor is calculated as:

$$I_L(peak) = I_{OUT}(max) + \frac{\Delta I_L}{2}$$

The saturation current rating of the inductor should exceed the peak inductor current (IL(peak)). It is advisable to select an inductor with a saturation current that is higher than the current limit set for the A7106H. Keep in mind that the saturation current levels of inductors typically decrease as the temperature rises.

Output Capacitor (C_{OUT})

The output capacitor limits the capacitive voltage ripple at the converter output. This voltage ripple which is generated from the triangular inductor current ripple flowing into and out of the capacitor can be calculated as:

$$\Delta V_{OUT} = \frac{\Delta I_L}{8 \times F_{sw} \times C_{OUT}}$$

The equation above only accounts for the steady-state ripple. It's also important to consider transient requirements when choosing the output capacitor. A ceramic capacitor rated X5R or higher, with a capacitance

greater than 22μF, is recommended. Additionally, for applications with high peak currents, an electrolytic capacitor larger than 100μF is also advised.

Enable Operation

Input UVLO can be programmed by EN rising threshold. The UVLO turn-on voltage can be calculated as:

$$V_{UVLO} = (1 + \frac{R_{EN1}}{R_{EN2}}) \times V_{ENH}$$

V_{ENH} is EN rising threshold voltage, typical is 1.17V.

The UVLO hysteresis is achieved using an internal 1.6μA current source that is turned on or off within the impedance of the set-point divider. When the voltage at the EN pin surpasses the rising threshold, the current source activates, rapidly increasing the voltage at the EN pin. The hysteresis can be calculated as follows:

$$V_{hys}(V) = R_{EN1} \times 1.6\mu A$$

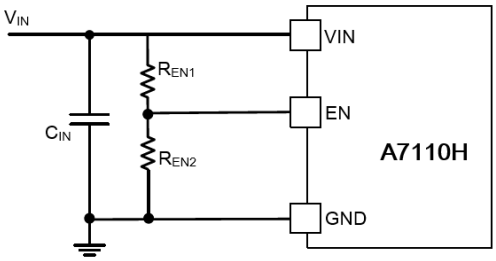


Fig 14. Enable Resistance Divider

Boot-strap capacitor

This capacitor supplies energy to the high-side gate driver. It is recommended to use a high-quality 10nF ceramic capacitor between the BOOT pin and the SW pin. Additionally, an RC series network can be employed to reduce the turn-on speed of the high-side MOSFET.

Power Good (PGOOD)

A7106H provides a PGOOD flag pin to indicate whether the output voltage is within the regulation level. PGOOD is an open-drain output that requires a pull-up resistor to a DC source. The typical range of pull-up resistance is about 10 kΩ. When the FB voltage exceeds 96% of the reference, the internal switch will be turned off, and PGOOD can be pulled high by the pull-up resistor. If the FB voltage falls below 92% of the reference, the switch will be turned on, and PGOOD is pulled low to indicate that the output voltage is out of regulation

APPLICATION AND IMPLEMENTATION

Reference Design1

Parameter	Symbol	Specification Value
Input Voltage	VIN	24V
Output Voltage	VOUT	5.0V
Switching Frequency	F_{SW}	320kHz (Typ.)
Maximum Output Current	$IOUT_{MAX}$	0.6A

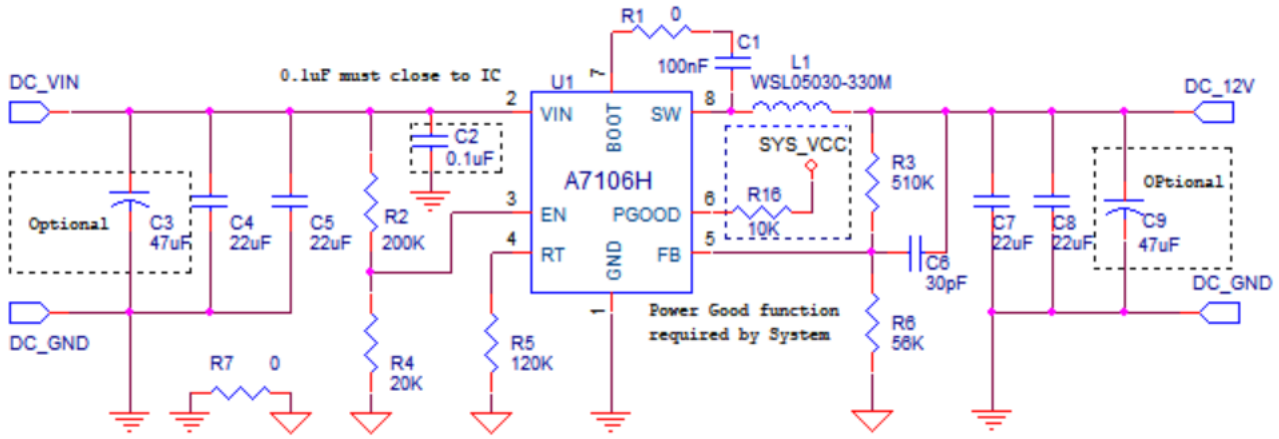


Fig 15. VOUT=12V Schematic

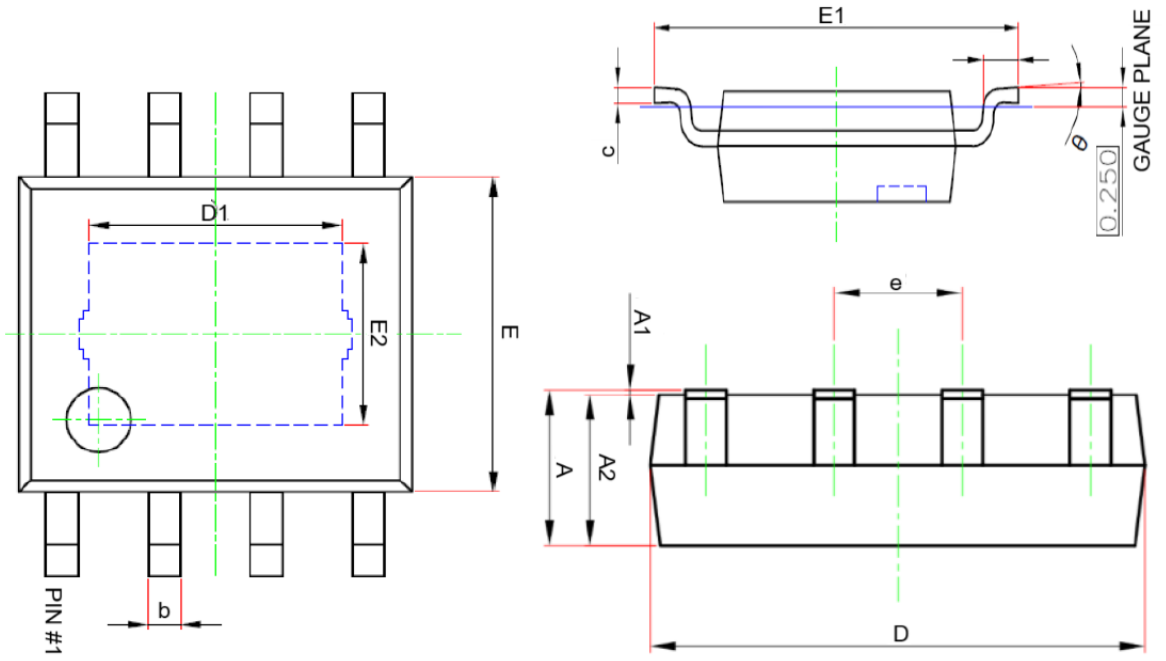
LAYOUT GUIDELINES

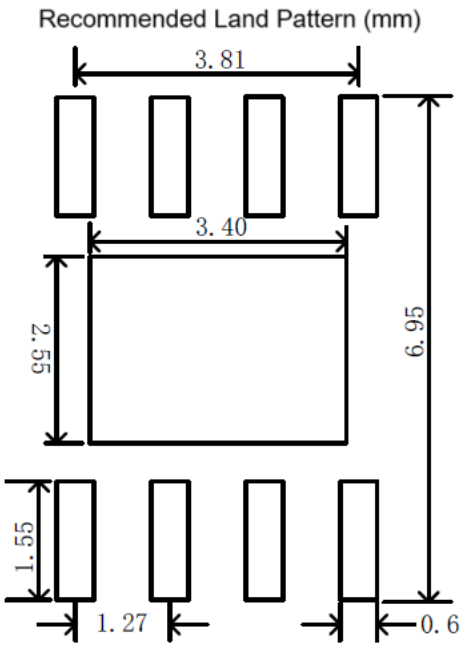
To ensure optimal performance of the A7106H, adhere to the following layout guidelines:

1. Use at least one low-ESR ceramic bypass capacitor (CIN). Position the CIN as close as possible to the VIN and GND pins of the A7106H, and place decoupling capacitors as near as possible between the VIN and the GND of the catch diode.
2. Reduce the loop area created by the connections of CIN to the VIN and GND pins.
3. Position the inductor close to the SW pin and minimize the area of the SW trace to prevent potential noise issues.
4. Optimize the PCB area around the GND pin and thermal pad. If possible, incorporate a ground plane to serve as both noise shielding and a heat dissipation pathway.
5. Position the feedback resistors, Rf1 and Rf2, near the FB pin. Ensure that the feedback VOUT sensing path is routed away from noisy areas, such as the SW net.
6. The RT pin is susceptible to noise, so the resistor for setting the on-time (RT) should be located close to the device.

PACKAGE INFORMATION

Dimension in PSOP8 (Unit:mm)





Symbol	Millimeters	
	Min	Max
A	1.300	1.700
A1	0.000	0.100
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
E	3.800	4.000
E1	5.800	6.200
D1	3.050	3.250
E2	2.160	2.360
e	1.270 BSC	
L	0.400	1.270
θ	0°	8°

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