DESCRIPTION

The AO1170-Q offers high voltage (32V), cost-optimized operation amplifier. AO1170-Q also offers strong general-purpose DC and AC specifications, including rail-to-rail output, low offset, low offset drift and 1.2MHz bandwidth.

Convenient features such as wide differential input voltage range, high output current, and high slew rate of 0.67V/us make the AO1170-Q a robust operational amplifier for high-voltage, cost-effective applications. as well as an excellent speed/power consumption ratio, providing an excellent bandwidth (1.2MHz) and slew rate of 0.67V/us. The op-amps are unity-gain stable and feature an ultra-low input bias current.

The AO1170-Q is stable at capacitance up to 300pF (Typ) and operation under single power supplies of 3V to 32V or dual power supplies of ±1.5V to ±16V.

The AO1170-Q is available in SOT-25, SOP8, MSOP8 and TSSOP8 package with AEC-Q100 qualified.

ORDERING INFORMATION

Package Type	Part Number	
SOT-25 SPQ: 3,000pcs/Reel	E5	AO1170E5VRQ-Z
SOP8 SPQ: 4000pcs/Reel	M8	AO1170M8VRQ
MSOP8 SPQ: 4000pcs/Reel	MS8	AO1170MS8VRQ
TSSOP8 SPQ: 4000pcs/Reel	TMX8	AO1170TMX8VRQ
Note	Z: Pin Description A or B V: Halogen free Package R: Tape & Reel Q: AEC-Q100 Qualified	
AiT provides all RoHS products		

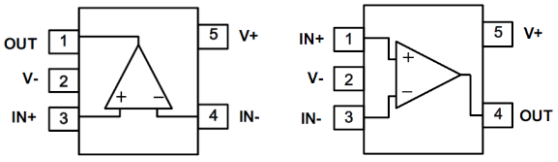
FEATURES

- AEC-Q100 Qualified for Automotive
- Low Offset Voltage: ±0.5mV (Typical)
- Low Offset Voltage Drift: ±3uV/°C
- Low Noise: 45nV/√Hz at 1kHz
- High Common-Mode Rejection Ratio: 110dB
- Low Bias Current: ±10pA
- Rail-to-Rail Output
- Wide Bandwidth:1.2MHz GBW
- High Slew Rate: 0.67V/us
- Low Quiescent Current: 120uA per Amplifier
- Supply Range: +3V to +32V ; ±1.5V to ±16V.

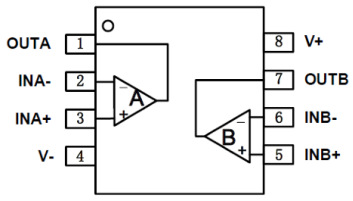
APPLICATION

- Merchant Network and Server PSU
- Industrial AC-DC & Merchant DC/DC
- Motor Drives: AC and Servo Drive Power Supplies
- Building Automation
- Sensors
- Photodiode Amplification
- Active Filters
- Test Equipment

TYPICAL APPLICATION

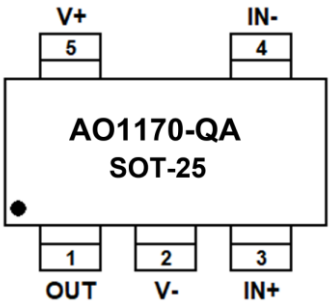


SOT-25-A SOT-25-B

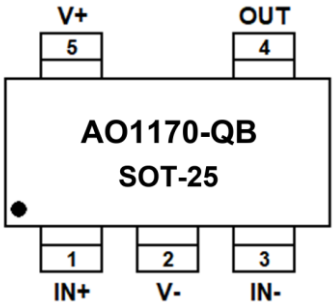


SOP8 / MSOP8 / TSSOP8

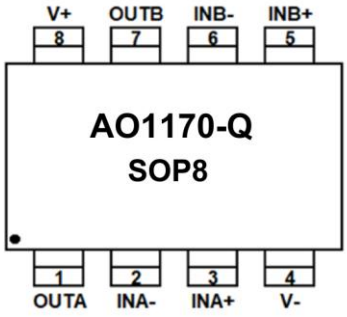
PIN DESCRIPTION



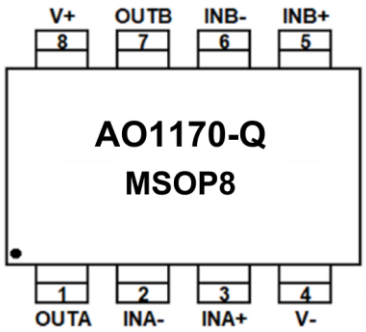
SOT-25, E5-A
Top View



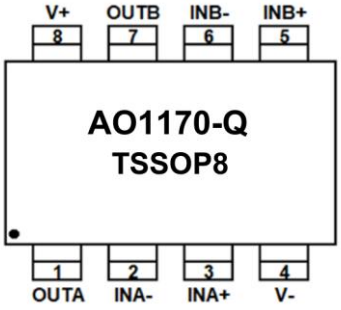
SOT-25, E5-B
Top View



SOP8, M8
Top View



MSOP8, MS8
Top View



TSSOP8, TMX8
Top View

Pin #			Symbol	I/O	Function
SOT-25		SOP8 MSOP8 TSSOP8			
A	B				
1	4	1,7	OUT	O	Output
2	2	4	V-	-	Negative (lowest) power supply or ground (for single supply operation)
3	1	3, 5	IN+	I	Positive (noninverting) input
4	3	2, 6	IN-	I	Negative (inverting) input
5	5	8	V+	-	Positive (highest) power supply

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range, unless otherwise noted

Supply Voltage, Vs=(V+) - (V-)		-0.7V ~ 36V
Signal Input Voltage Pin NOTE1		(V-)-0.2V ~ (V+)0.2V
Signal Output Voltage Pin NOTE2		(V-)-0.2V ~ (V+)0.2V
Signal Input Current Pin NOTE1		-10mA ~ 10mA
Signal Output Current Pin NOTE2		-100mA ~ 100mA
Output Short-Circuit Current NOTE3		Continuous
T_A, Operating Range Temperature		-40℃ ~ 125℃
T_J, Junction Temperature		150℃
T_{STG}, Storage Temperature		-55℃ ~ 150℃
ESD Ratings NOTE4		
$V_{(ESD)}$, Electrostatic discharge	Human-body model (HBM), Per AEC-A100-002 NOTE5	±2000V
	Charged-Device Model (CDM) Per AEC-Q100-011	±200V
	Latch-UP (LU), Per AEC-Q100-004	±100mA

Stress beyond above above-listed “Absolute Maximum Ratings” may lead to permanent damage to the device. These are stress ratings only, and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

NOTE 1: Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current-limited to 10mA or less.

NOTE 2: Output terminals are diode-clamped to the power-supply rails. Output signals that can swing more than 0.5V beyond the supply rails should be current-limited to ±100mA or less.

NOTE 3: Short-circuit to ground, one amplifier per package.

NOTE 4: JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

NOTE 5: AEC Q100-002 indicates that HBM stressing shall follow the ANSI/ESDA/JEDEC JS-001 specification.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, unless otherwise noted

Parameter		Min.	Typ.	Max.	Unit
Supply voltage Vs= (V+) - (V-)	Single-Supply	3	-	32	V
	Dual-Supply	±1.5	-	±16	

ELECTRICAL CHARACTERISTICS

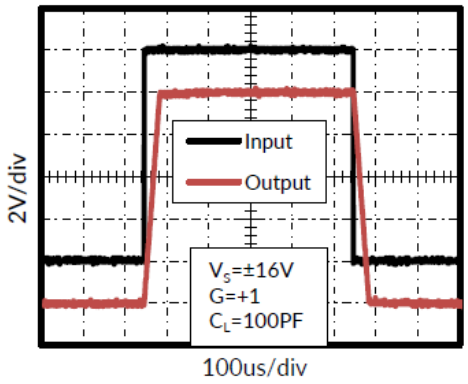
T_A = +25°C, V_S=3V to 32V, R_L = 10kΩ connected to V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

Parameter	Symbol	Conditions	T_J	Min	Typ	Max	Units
POWER SUPPLY							
Operating Voltage Range	Vs		+25°C	3	-	32	V
Quiescent Current/Amplifier	I_Q	V_S=±2.5V, Io=0mA	+25°C	-	120	280	uA
		V_S=±16V, Io=0mA		-	175	340	
Power-Supply Rejection Ratio	PSRR	V_S=5V to 36V	+25°C	98	120	-	dB
INPUT							
Input Offset Voltage	Vos	V_{CM}=V_S/2	+25°C	-2	±0.5	2	mV
			-40°C to 125°C	-3	-	3	
Input Offset Voltage Average Drift	Vos Tc		-40°C to 125°C	-	±3	-	uV/°C
Input Bias Current	I_B	V_{CM}=V_S/2	+25°C	-	±10	-	pA
Input Offset Current	I_{OS}	V_{CM}=V_S/2	+25°C	-	±10	-	pA
Common-Mode Voltage Range	V_{CM}	V_S=±16V	-40°C to 125°C	(V-)-0.1	-	(V+)-2	V
Common-Mode Rejection Ratio	CMRR	V_S=±16V, V_{CM}=(V-)-0.1V to (V+)-2V	+25°C	100	110	-	dB
		V_S=±18V, V_{CM}=(V-)-0.1V to (V+)-2V	-40°C to 125°C	90	-	-	
OUTPUT							
Open-Loop Voltage Gain	A_{OL}	RL=10KΩVo=(V-)+0.6V to (V+)-0.6V	+25°C	83	115	-	dB
Output Swing	V_{OH}	V_S=±16V, R_L=10KΩ	+25°C	-	-	-17.85	V
	V_{OL}		+25°C	-	70	-	V
Short-Circuit Current	I_{SC}		+25°C	±35	±80	-	mA
Capacitive Load Drive	C_{LOAD}		+25°C	-	100	-	pF
FREQUENCY RESPONSE							
Slew Rate	SR	G=+1, C_L=100pF	+25°C	-	0.67	-	V/us
Gain-Bandwidth Product	GBW		+25°C	-	1.2	-	MHz
Setting Time,0.01%	ts	V_S=±2.5V, G=+1, C_L=100pF, Step=2V	+25°C	-	5	-	us
Overload Recovery Time	t_{OR}	V_{IN}·Gain≥V_S, G=11	+25°C	-	5	-	us
Turn On Time	t_{ON}		+25°C	-	10	-	us
NOISE							
Input Voltage Noise	En	f=0.1Hz to 10Hz, Vs=±2.5V	+25°C	-	16	-	uVpp
Input Voltage Noise Density	en	f=1KHz			45		nV/√Hz

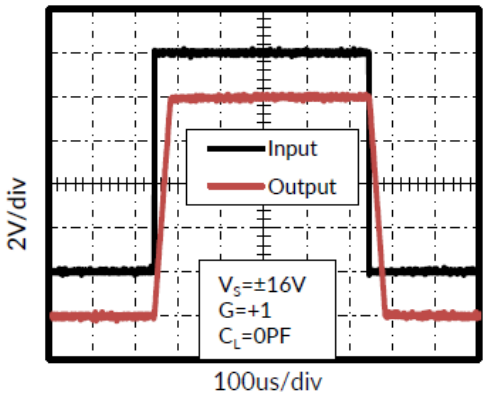
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25°C, V_S=±16V, R_L = 10kΩ connected to V_S/2, V_{OUT} = V_S/2, unless otherwise noted.

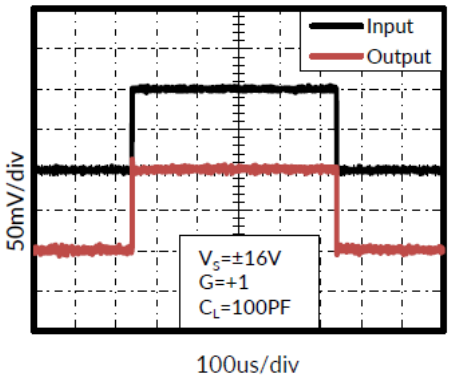
1. Large Signal Step Response



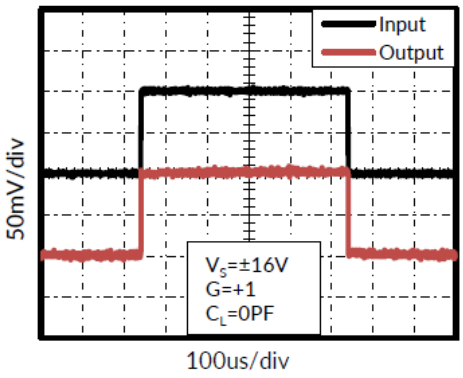
2. Large Signal Step Response



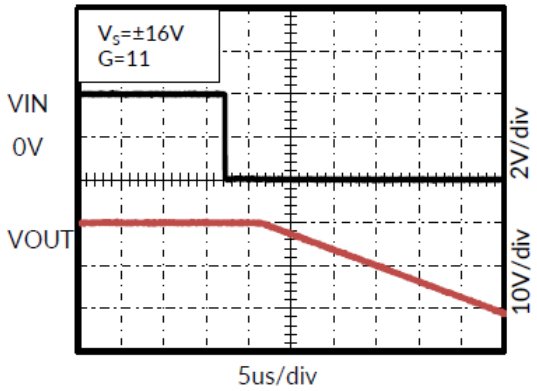
3. Small Signal Step Response



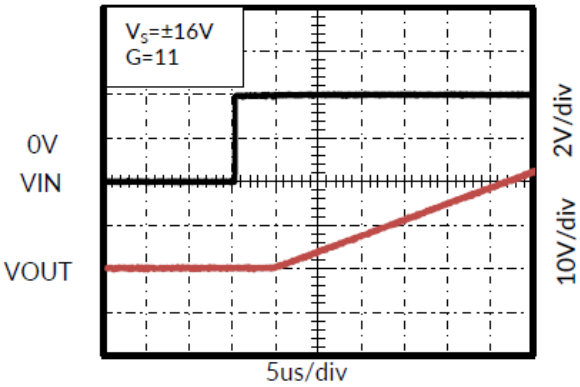
4. Small Signal Step Response



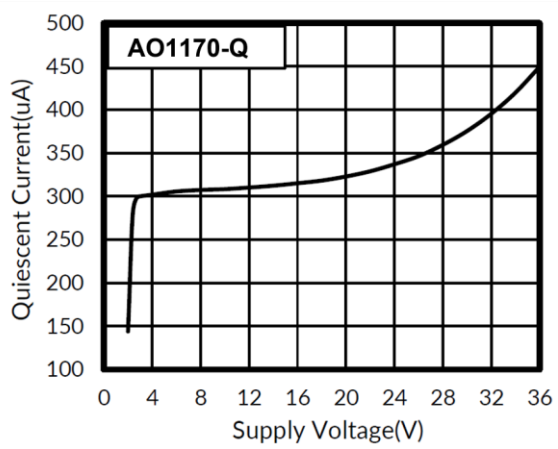
5. Negative Overvoltage Recovery



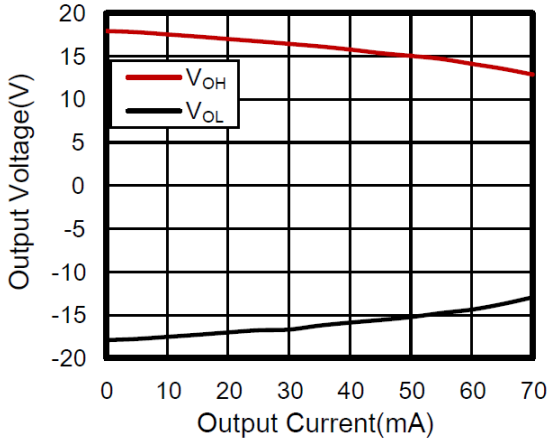
6. Positive Overvoltage Recovery



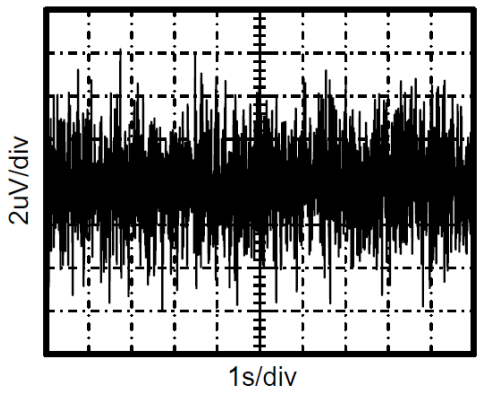
7. Quiescent Current vs Supply Voltage



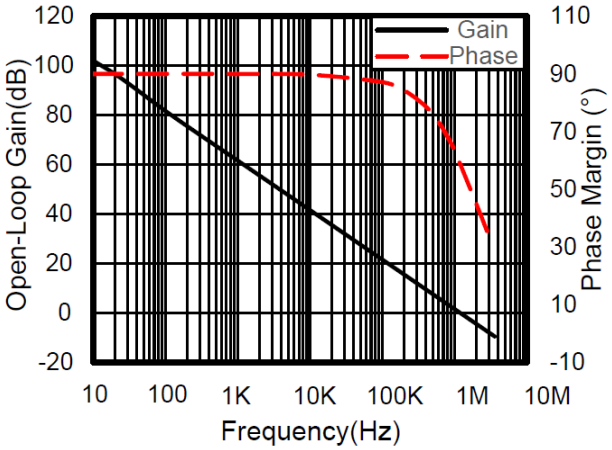
8. Output Voltage Swing vs Output Current



9. 0.1Hz to 10Hz Noise at V_S=5V



10. Open-Loop Gain and Phase vs. Frequency



DETAILED DESCRIPTION

The AO1170-Q single-supply CMOS operational amplifiers provide rail-to-rail input and output capability with 1.2-MHz bandwidth. Consuming a μA consumption and the AO1170-Q is the perfect choice for portable and battery-operated applications. The maximum recommended supply voltage is 32 V, which allows the devices to be operated from (±16 V supplies down to ±1.5 V) a variety of rechargeable cells. The rail-to-rail inputs with high input impedance make the AO1170-Q ideal for sensor signal-conditioning applications, etc.

Rail to Rail Input Operation

The AO1170-Q input stage consists of two differential transistor pairs that operate together to achieve rail-to-rail input operation. As the common-mode input voltage approaches the positive supply rail, the input pair switches from the PMOS differential pair to the NMOS differential pair. This transition occurs approximately 1.5 V from the positive rail and results in a change in offset voltage due to different device characteristics between the NMOS and PMOS pairs. If the input signal to the device is large enough to swing between both rails, this transition results in a reduction in common-mode rejection ratio (CMRR). If the input signal does not swing between both rails, it is best to bias the signal in the region where only one input pair is active, where the offset voltage varies slightly across the input range, and optimal CMRR can be achieved.

Driving a Capacitive Load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin, leading to high-frequency ringing or oscillations. Therefore, for capacitive loads greater than 10 pF, it is recommended that a resistor be placed in series (R_{NULL}) to stabilize the output of an operational amplifier. R_{NULL} modifies the open-loop gain of the system to ensure that the circuit has sufficient phase margin, as shown in Figure 1. A minimum value of 20 Ω should work well for most applications.

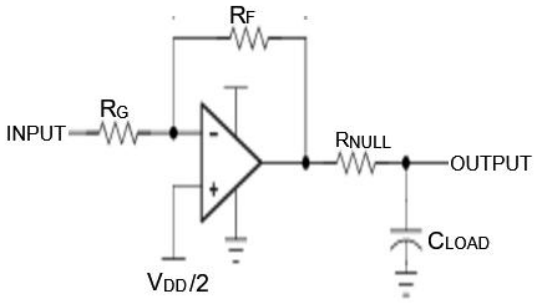


Figure 1 . Driving a Capacitive Load

Application Information

When designing for low power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors can react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations can affect the stability of the overall system. Use of a feedback capacitor assures stability and limits overshoot or gain peaking.

Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in Figure 2. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative input voltages positive on the output. In addition, amplification can be added by selecting the input resistor R_I and the feedback resistor R_F.

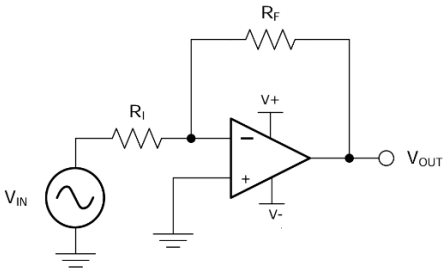


Figure 2. Application Schematic

Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range (V_{CM}) and the output voltage swing to the rails (V_O) must also be considered.

• Supply voltage: 30 V (±15 V)

• Capacitive loads: 100 pF, 1000 pF, 0.01μF, 0.1μF, and 1μF

• Phase margin: 45° and 60°

Detailed Design Procedure

Figure 1 shows a unity-gain buffer driving a capacitive load. Equation 1 shows the transfer function for the circuit in Figure 1. Figure 1 does not show the open-loop output resistance of the operational amplifier (Ro).

$$T(s) = (1+C_{LOAD}\times R_{NULL}\times S) / (1+(R_O+R_{NULL})\times C_{LOAD}\times S) \quad (1)$$

The transfer function in Equation 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_O +R_{NULL}) and C_{LOAD}. The R_{NULL} and C_{LOAD} components determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{NULL} so that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1/β is 20 dB per decade.

Layout Guideline:

To achieve the levels of high performance of the AO1170-Q, follow the proper printed circuit board design techniques. A general set of guidelines is given below.

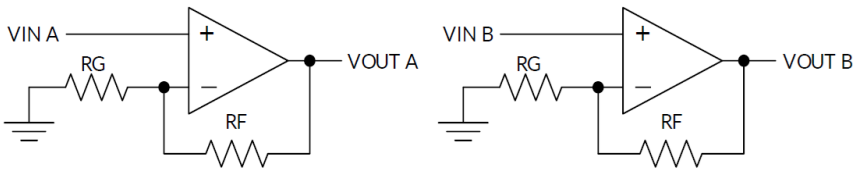
• **Ground planes**— it is highly recommended to use a ground plane on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and outputs, the ground plane can be removed to minimize stray capacitance.

• **Short trace runs and compact part placements**—Optimum high performance is achieved when stray series inductance has been minimized. To realize this, the circuit layout must be made as compact as possible, thereby minimizing the length of all trace runs. Pay particular attention to the inverting input of the amplifier. Its length must be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.

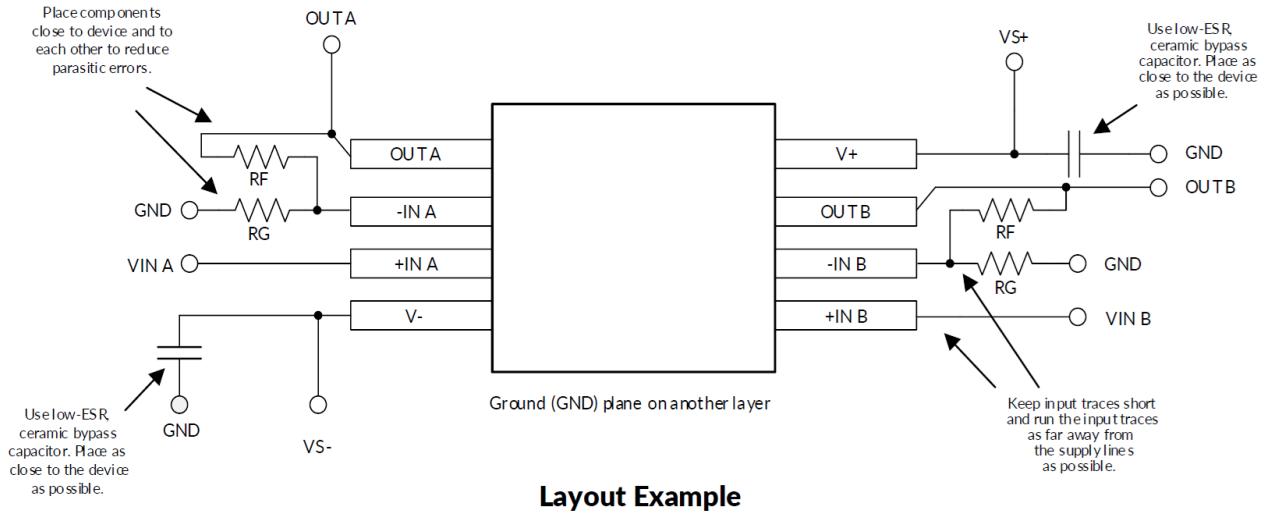
• **Proper power supply decoupling**—Use a large tantalum capacitor in parallel with a 0.1-μF bypass ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF bypass ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF by pass capacitor must be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer should strive for distances of less than 0.1 inches between the device power terminals and the ceramic capacitors.

• **Surface-mount passive components**—Using surface-mount passive components is recommended for high-performance amplifier circuits for several reasons. First, because of the extremely low lead inductance of surface-mount components, the problem with stray series inductance is greatly reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, thereby minimizing both stray inductance and capacitance. If lead components are used, it is recommended that the lead lengths be kept as short as possible.

Layout Example:



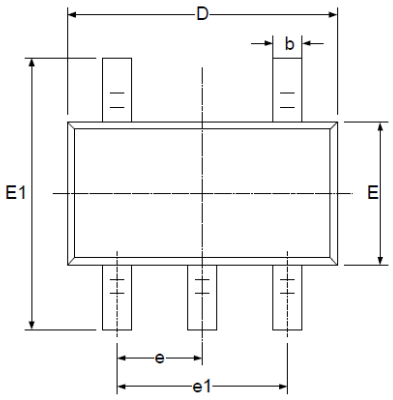
Schematic Representation

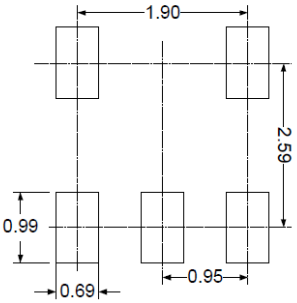


Layout Example

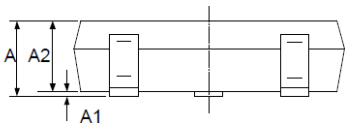
PACKAGE INFORMATION

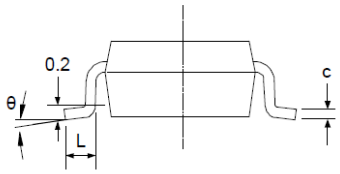
Dimension in SOT-25 (Unit: mm/ inch)





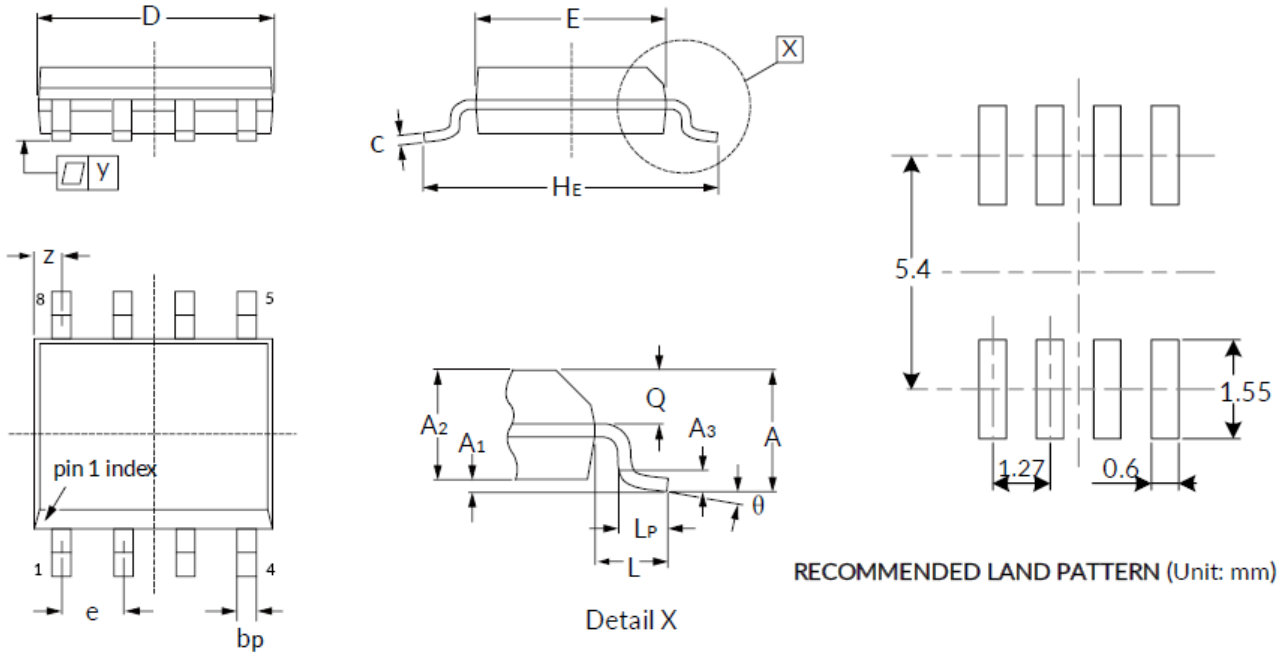
RECOMMENDED LAND PATTERN (Unit: mm)





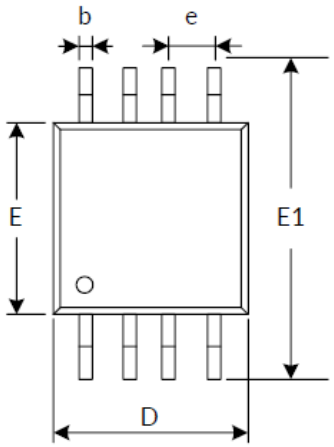
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 BSC		0.037 BSC	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

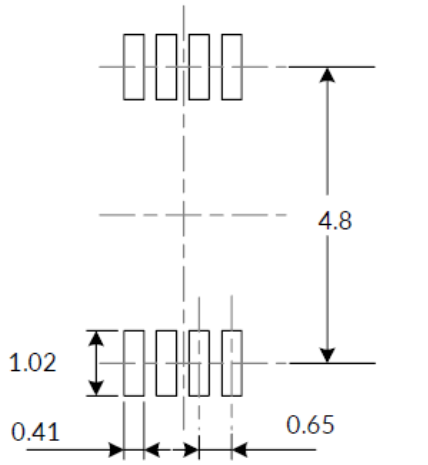
Dimension in SOP8 (Unit: mm/ inch)



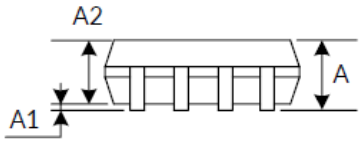
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.750		0.069
A_1	0.100	0.250	0.004	0.010
A_2	1.250	1.450	0.049	0.057
A_3	0.250		0.010	
b_p	0.360	0.490	0.014	0.019
c	0.190	0.250	0.007	0.010
D (1)	4.800	5.000	0.190	0.200
E (1)	3.800	4.000	0.150	0.160
H_E	5.800	6.200	0.228	0.244
e	1.270		0.050	
L	1.050		0.041	
L_P	0.400	1.000	0.016	0.039
Q	0.600	0.700	0.024	0.028
Z	0.300	0.700	0.012	0.028
y	0.100		0.004	
θ	0°	8°	0°	8°

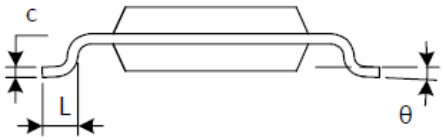
Dimension in MSOP8 (Unit: mm/ inch)





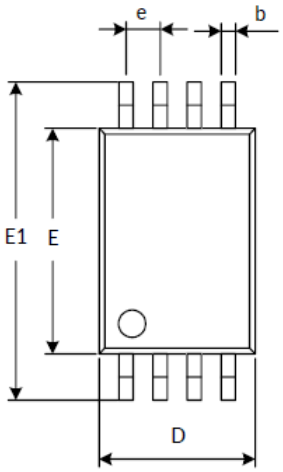
RECOMMENDED LAND PATTERN (Unit: mm)

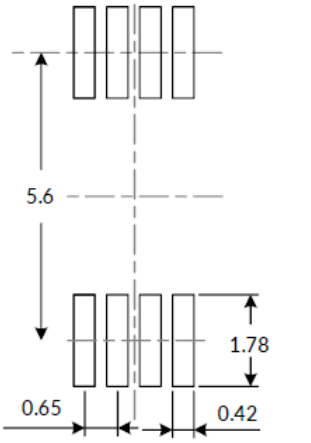




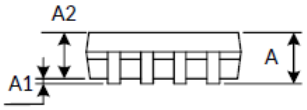
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D (1)	2.900	3.100	0.114	0.122
e	0.650(BSC) (2)		0.026(BSC) (2)	
E (1)	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

Dimension in TSSOP8 (Unit: mm/ inch)





RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.900	1.050	0.035	0.041
b	0.200	0.280	0.008	0.011
c	0.130	0.170	0.005	0.007
D (1)	2.900	3.100	0.114	0.122
E (1)	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650(BSC) (2)		0.026(BSC) (2)	
L	0.450	0.750	0.018	0.030
H	0.250(TYP)		0.010(TYP)	
θ	0°	8°	0°	8°

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