DESCRIPTION

The AC1042 is a high-speed, fault-tolerant CAN transceiver that serves as the interface between a CAN (Controller Area Network) protocol controller and the physical two-wire CAN bus. It provides differential transmit and receive capabilities and is fully compliant with ISO 11898-2 and ISO 11898-5 standards.

The AC1042 supports direct interfacing with microcontrollers operating from 1.8V to 5.5V supply voltages. When the supply is off, the transceiver exhibits a passive behavior on the CAN bus, ensuring minimal disruption to the network.

Key features include Low-current standby mode with bus wake-up capability, and support for CAN FD communication with data rates up to 5 Mbit/s during the fast phase. The AC1042 is ideal for applications requiring high-speed, robust CAN communication with energy-efficient operation and extended compatibility.

The AC1042 is available in SOP-8 package.

ORDERING INFORMATION

Package Type	Part Number	
SOP8 SPQ:4,000pcs/Reel	M8	AC1042M8R-A
		AC1042M8VR-A
		AC1042M8R-B
		AC1042M8VR-B
Note	A, B: Pin Assignment V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

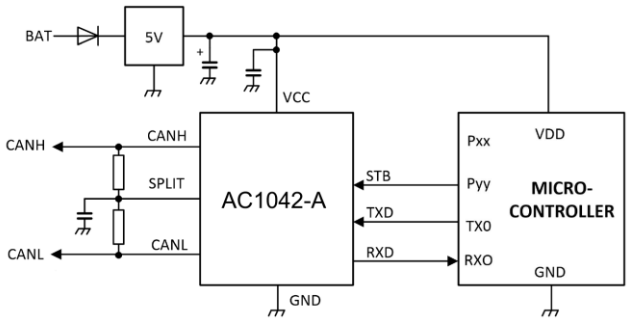
FEATURES

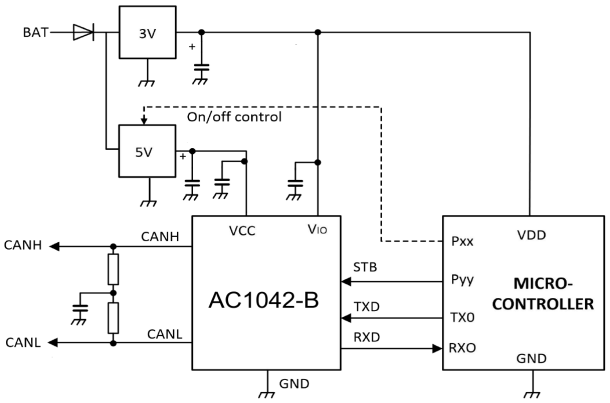
- Very Low standby current (5 μA , typical)
- VIO Supply pin to interface directly to CAN
- Controllers and MCU with 1.8V to 5.5V I/O
- SPLIT output pin to stabilize common mode in biased split termination schemes.
- CAN bus pins are disconnected when device is unpowered
- Bus glitch-free power-up and power-down
- Over temperature protection
- Allow up to 128 transceivers on the bus
- Data rate up to 5Mbps
- Half-duplex transceiver

APPLICATION

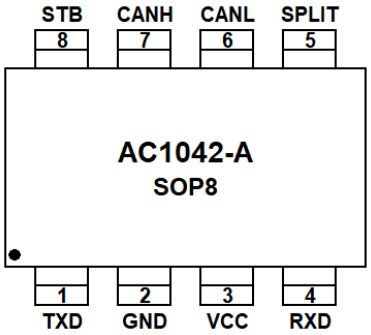
- Industrial Automation, Control
- CAN Networks

TYPICAL APPLICATION

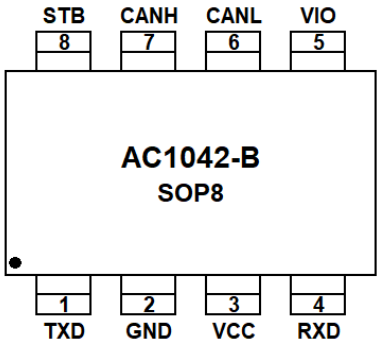




PIN DESCRIPTION



SOP8, M8
Type A
Top View



SOP8, M8
Type B
Top View

Pin #		Symbol	Function
Type A	Type B		
1	1	TXD	Transmit digital data input. LOW for dominant and HIGH for recessive bus states.
2	2	GND	Ground
3	3	V_{CC}	Supply Voltage
4	4	RXD	Receive digital data output; reads out data from the bus lines, LOW for dominant and HIGH for recessive bus states.
5	-	SPLIT	Common-mode stabilization output; in AC1042-A version only
-	5	VIO	Supply voltage for I/O level adapter; in AC1042-B version only
6	6	CANL	Low-level CAN bus I/O line
7	7	CANH	High-level CAN bus I/O line
8	8	STB	Standby mode control input (Active high)

ABSOLUTE MAXIMUM RATINGS

V_{CC}, DC Supply Voltage		-0.3V ~ +7V
V_{IO}, IO level DC Supply Voltage		-0.3V ~ +7V
DC Voltage at TXD, RXD, STB		-0.3 ~ V_{IO}+0.3V
DC Voltage at CANH, CANL and SPLIT		-44V ~ +44V
RXD Output Current		-8mA ~ +8mA
Operating Junction Temperature		-40°C ~ +125°C
Storage Temperature		-55°C ~ +150°C
Package Thermal Resistance	SOP8	150°C/W

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	-	4.5	5	5.5	V
Supply Voltage on Pin V_{IO}	V_{IO}	-	2.8	3.3	5.5	V
Operating Ambient Temperature	-	-	-40	-	85	°C
Operating Junction Temperature	-	-	-40	-	125	°C

DC Characteristics

At V_{CC} = 4.5V ~ 5.5V, T_A=25°C, V_{IO}=2.8V ~ 5.5V, R_L=60Ω, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VCC Supply						
Voltage Range	V_{CC}	-	4.5	5	5.5	V
Under Voltage Detection Voltage	V_{UVD}	-	3.5	4	4.5	V
Hysteresis of UVD Comparator	V_{UVDH}	-	0.3	0.5	0.8	V
Supply Current	I_{CC}	Recessive; $V_{TXD}=V_{IO}$	-	4	10	mA
		Dominant; V_{TXD}=0V	-	22	40	
Open Loop Voltage Gain	I_{CCS}	AC1042-A	-	12	17	µA
		AC1042-B	-	-	1	
V_{IO} Supply						
Digital Supply Voltage Range	V_{IO}	-	2.8	-	5.5	V
Undervoltage Detection Voltage	V_{UVIO}	-	1.4	2	2.7	V
Supply Current	I_{VIO}	Normal mode; V_{TXD}=0 or V_{IO}	-	20	200	µA
		Standby mode	-	12	17	
BUS Line (CANH; CANL) Transmitter						
Standby Mode Output Voltage	$V_{O(S)}$	Standby mode, no load	-0.1	0	+0.1	V
Recessive Output Voltage	$V_{O(R)}$	Normal mode, $V_{TXD}=V_{IO}$, no load	2	0.5V_{CC}	3	mV
Recessive, Differential Output Voltage	$V_{O(DIFF)}$	$V_{TXD}=V_{IO}$	-50	0	50	mV
		$V_{TXD}=V_{IO}$, no load	-500	0	50	
Recessive, Short Circuit Output Current	$I_{O(SC)}$	Normal mode, $V_{CANH}=V_{CANH}$=-27V to +32V	-5		+5	mA
Dominant Output Voltage	$V_{O(D)}$	Pin CANH, V_{TXD}=0V	2.75	3.5	4.5	V
		Pin CANL, V_{TXD}=0V	0.5	1.5	2.25	
Dominant, Differential Output Voltage	$V_{O(DIFF)}$	Dominant, Normal mode, V_{TXD}=0V	1.5	2.0	3.0	V
Dominant Output Voltage Symmetry	$V_{O(D)(M)}$	V_{DD}-V_{CANH}-V_{CANL}	-400	0	400	mV
Dominant Short Circuit Output Current	$I_{O(SC)}$	C_{ANH}; V_{TXD}=0, V_{CANH}=0V	-120	-70	-40	mA
		C_{ANL}; V_{TXD}=0, V_{CANL}=18V	40	85	120	
BUS Line (CANH; CANL) Receiver						
Recessive Differential Input Voltage	$V_{DIFF(RI)}$	Normal mode; -12V ≦ $V_{CANH,CANL}$ ≦ +12V;	-1.0	-	+0.5	V
		Standby mode; -12V ≦$V_{CANH,CANL}$≦+12V;	-1.0	-	+0.4	V
Dominant Differential Input Voltage	$V_{DIFF(DI)}$	Normal mode; -12V ≦ $V_{CANH,CANL}$ ≦ +12V;	0.9	-	V_{DD}	V
		Standby mode; -12V ≦ $V_{CANH,CANL}$ ≦ +12V;	1.0	-	V_{DD}	V
Differential Receiver Threshold	$V_{TH(DIFF)}$	Normal mode; -12V ≦ $V_{CANH,CANL}$ ≦+12V;	0.5	0.7	0.9	V
		Standby mode; -12V ≦ $V_{CANH,CANL}$ ≦ +12V;	0.4	-	1.15	V
Differential Input Hysteresis	$V_{HYS(DIFF)}$	Normal mode	50	-	200	mV
Common Mode Input Resistance	R_{IN}	-	10	15	25	kΩ
Common Mode Resistance Matching	$R_{IN(M)}$	-	-1	-	+1	%
Differential Input Resistance	$R_{IN(DIFF)}$	-	20	30	50	kΩ

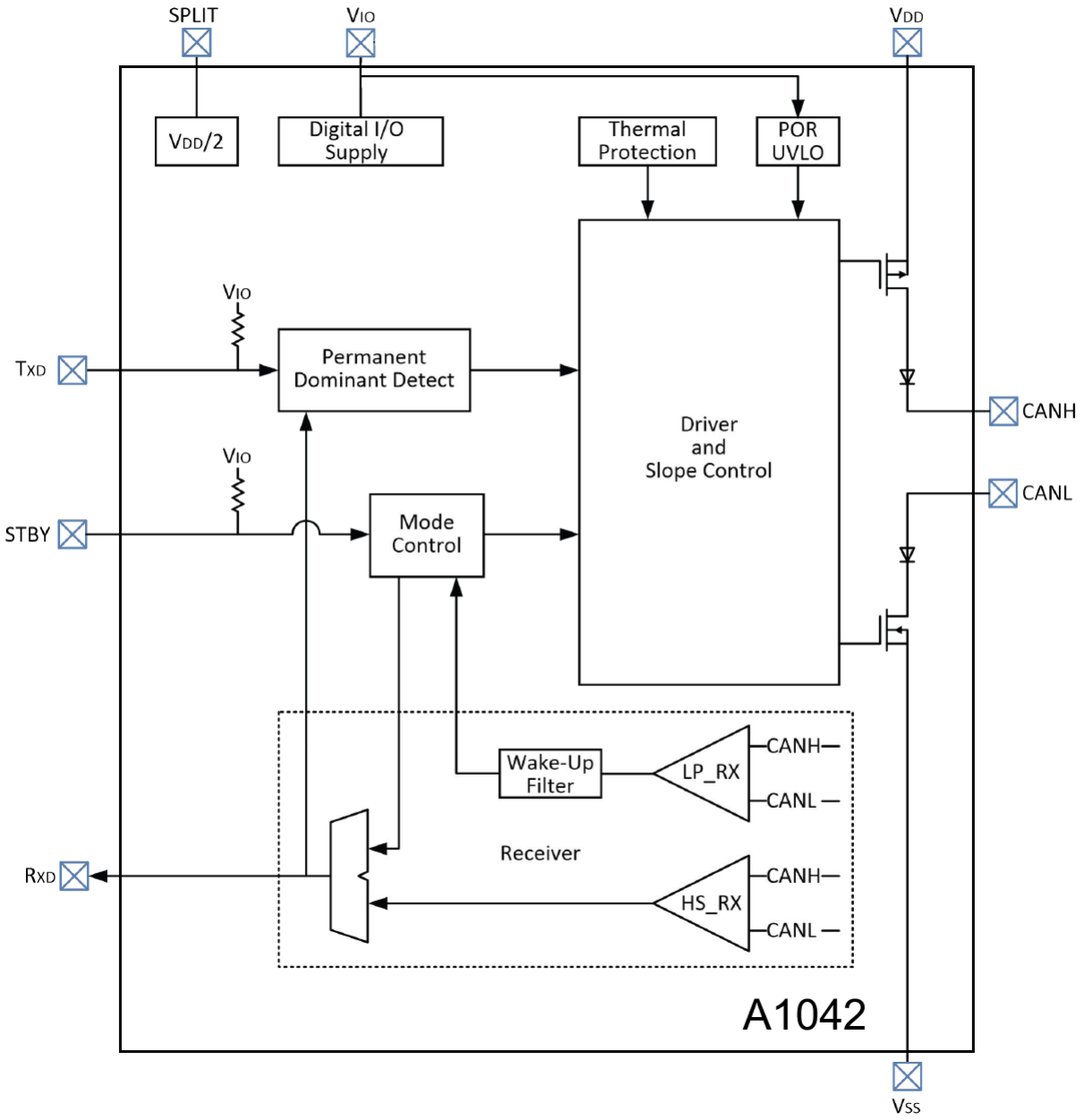
Common Mode Input Capacitance	$C_{IN(CM)}$	-	-	-	20	pF
Differential Input Capacitance	$C_{IN(DIFF)}$	-	-	-	10	pF
Input Leakage Current	I_{LI}	V_{CC} = V_{TXD} = V_{STB} = 0V; V_{CANH} = V_{CANL} = 5V	-5	-	+5	µA
SPLIT; Common Mode Stabilization Output Pin (only for AC1042-A)						
Output Voltage	V_O	Normal mode; I_{SPLIT} = -500µA to +500µA	0.3V_{CC}	0.5V_{CC}	0.7V_{CC}	V
		Normal mode; R_L = 1MΩ	0.45V_{CC}	0.5V_{CC}	0.55V_{CC}	V
Leakage Current	I_L	Standby mode; V_{SPLIT} = -24V to +24V	-5	-	+5	µA
TXD, STB Digital Input Pin						
High-Level Input Voltage	V_{IH}		0.7V_{IO}	-	V_{IO}+0.3	V
Low-Level Input Voltage	V_{IL}		-0.3	-	0.3V_{IO}	V
High-Level Input Current	I_{IH}		-1		+1	µA
TX: Low-Level Input Current	$I_{IL(TXD)}$		-270	-150	-30	µA
STB: Low-Level Input Current	$I_{IL(STB)}$		-20	-	-1	µA
RXD Receive Data Output Pin						
High-Level Output Voltage	V_{OH}	I_{OH}=-4mA	V_{IO}-0.4	-	-	V
Low-Level Output Voltage	V_{OL}	I_{OL}=4mA	-	-	0.4	V
Thermal Shutdown						
Shutdown, Junction Temperature	$T_{J(SD)}$	-	160	170	180	°C
Shutdown, Temperature Hysteresis	$T_{J(HYST)}$	-	20	30	40	°C

Dynamic Characteristics

T_A=25 °C, V_{CC}=4.5V to 5.5V, V_{IO}=1.8V to 5.5V, R_L=60Ω (Unless otherwise specified. See Figure 4,5,6)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Delay TXD Low to bus dominant	$t_{TXD-BUSON}$	Normal mode	-	65	-	ns
Delay TXD High to bus recessive	$t_{TXD-BUSOFF}$	Normal mode	-	60	-	ns
Delay bus dominant to RXD	$t_{BUSON-RXD}$	Normal mode	-	65	-	ns
Delay bus recessive to RXD	$t_{BUSOFF-RXD}$	Normal mode	-	65	-	ns
Propagation delay TXD Low to RXD Low	$t_{TXDL-RXDL}$	Normal mode	-	-	220	ns
Propagation delay TXD High to RXD High	$t_{TXDH-RXDH}$	Normal mode	-	-	220	ns
Bus wake-up filter time	$t_{FLTR(WAKE)}$	Standby mode	0.5	1	4	µs
Delay standby to normal mode	t_{WAKE}	Negative edge on STB	2	3	10	µs
TXD dominant time-out time	$T_{to(dom)TXD}$	V_{TXD}=0V, Normal mode	0.3	2	5	ms
Bus dominant time-out time	$T_{to(dom)BUS}$	Standby mode	0.3	2	5	ms

FUNCTION BLOCK DIAGRAM



Note

1: A1042-A has the SPILT pin

2: A1042-B has the V_{IO} pin

DETAILED INFORMATION

Operating Mode

AC1042 supports two operating modes, Normal and Standby, which are selected via pin STB. See Table1 for a description of the operating modes under normal supply conditions.

Table1

Mode	STB	DRIVER	RECEIVER	RXD	
				LOW	HIGH
Normal	LOW	Enable (ON)	Enable (ON)	Bus Dominant	Bus Recessive
Standby	HIGH		Only Low Power Bus Monitor is Active	Wake-Up Request Detected	No Wake-Up Request Detected

Normal Mode

A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME.

Standby Mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states but ensures that only bus dominant and bus recessive states that persist longer than tfltr(wake)bus are reflected on pin RXD. In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by VIO and is capable of detecting CAN bus activity even if VIO is the only supply voltage available. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.

Fail-Safe Features

TXD Dominant Time-out Function

A TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than tto(dom)TXD, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant

state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set to HIGH. The TXD dominant time-out time also defines the minimum possible bit rate of 40 kbit/s.

Bus Dominant Time-out Function

In Standby mode a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than tto(dom)bus, the RXD pin is reset to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

Internal Biasing of TXD and STB Input Pins

Pins TXD and STB have internal pull-ups to VIO to ensure a safe, defined state in case one or both pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize standby current.

Undervoltage Detection on Pins Vcc and VIO

Should VCC drop below the VCC undervoltage detection level, VUVD(VCC), the transceiver will switch to Standby mode. The logic state of pin STB will be ignored until VCC has recovered. Should VIO drop below the VIO undervoltage detection level, VUVD(VIO), the transceiver will switch off and disengage from the bus (zero load) until VIO has recovered.

Over-temperature Protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, Tj(sd), the output drivers will be disabled until the virtual junction temperature falls below Tj(sd) and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillation due to temperature drift is avoided.

Unpowered Device

The AC1042 is designed to be “ideal passive” or “no load” to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered to avoid loading down the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains in operation. The logic terminals also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

Floating Terminals

The AC1042 has internal pull ups on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to VCC or VIO to force a recessive input level if the terminal floats. The STB terminal is also pulled up to force the device into low power Standby mode if the terminal floats.

CAN Bus Short Circuit Current Limiting

The AC1042 has The device has two protection features that limit the short circuit current when a CAN bus line is short-circuit fault condition: driver current limiting (both dominant and recessive states) and TXD dominant state time out to prevent permanent higher short circuit current of the dominant state during a system fault.

SPLIT Output Pin and VIO Supply Pin

Two versions of the AC1042 are available, only differing in the function of a single pin. Pin 5 is either a SPLIT output pin or a VIO supply pin. Using the SPLIT pin on the AC1042-A in conjunction with a split termination network (see Figure 1 and Figure 2) can help to stabilize the recessive voltage level on the bus. This will reduce EME in networks with DC leakage to ground (e.g. from deactivated nodes with poor bus leakage performance). In Normal mode, pin SPLIT delivers a DC output voltage of 0.5VCC. In Standby mode or when VCC is off, pin SPLIT is floating. When not used, the SPLIT pin should be left open.

Pin V_{IO} on the AC1042-B should be connected to the micro-controller supply voltage (see Figure 3). This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the micro-controller. Pin VIO also provides the internal supply voltage for the low-power differential receiver of the transceiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin VCC. For versions of the AC1042 without a VIO pin, the VIO input is internally connected to VCC. This sets the signal levels of pins TXD, RXD and STB to levels compatible with 5 V micro-controllers.

Fig 1. Stabilization Circuitry and Application for Version with SPLIT Pin

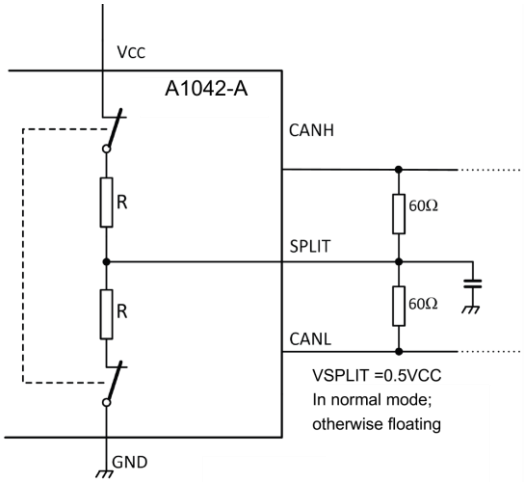


Fig 2. Typical Application with AC1042-A and a 5V Micro-controller

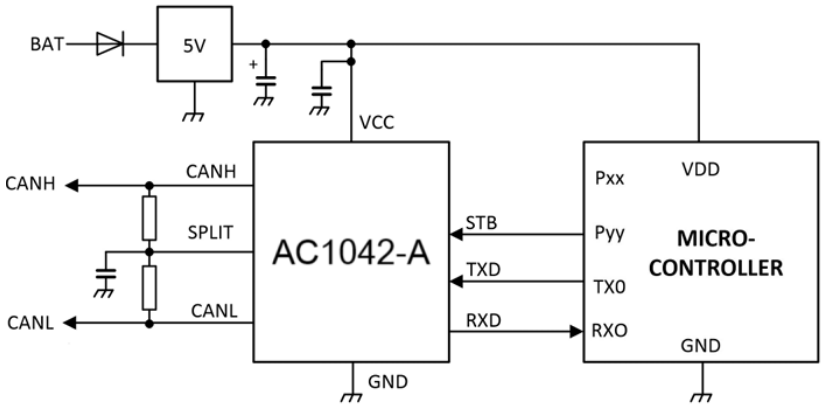


Fig 3. Typical Application with AC1042-B and a 3V Micro-controller

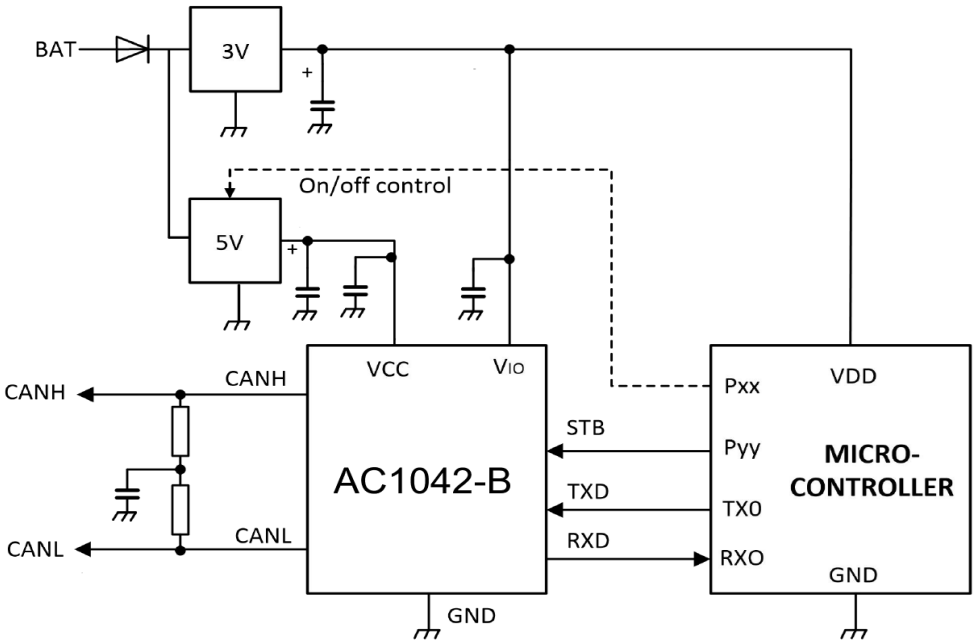


Fig 4. Test Circuit for Measuring Transceiver Driver Symmetry

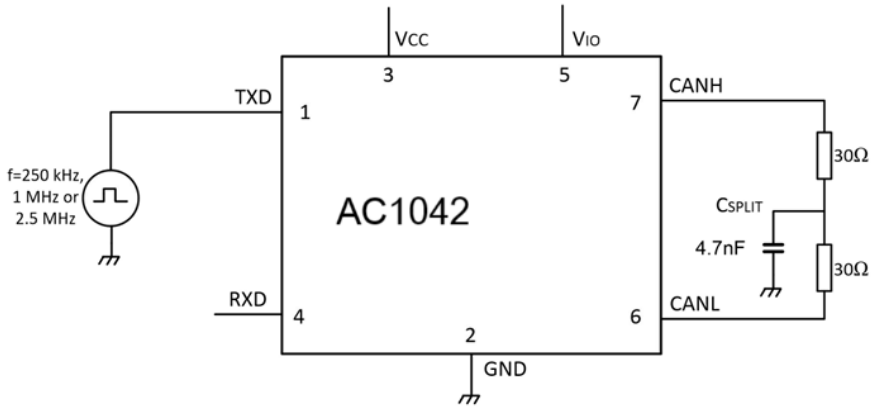


Fig 5. CAN Transceiver Timing Diagram

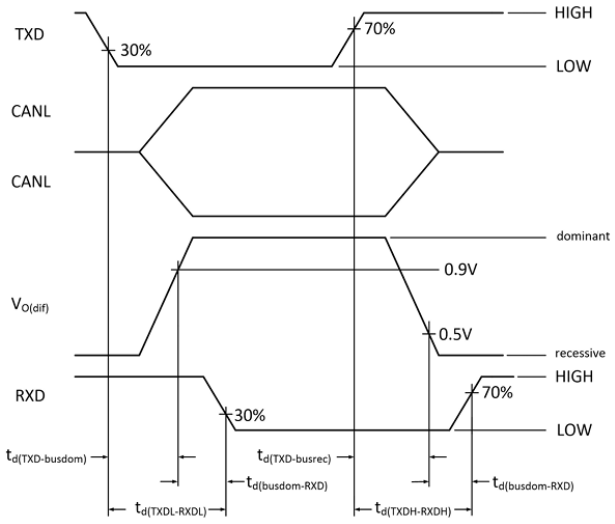
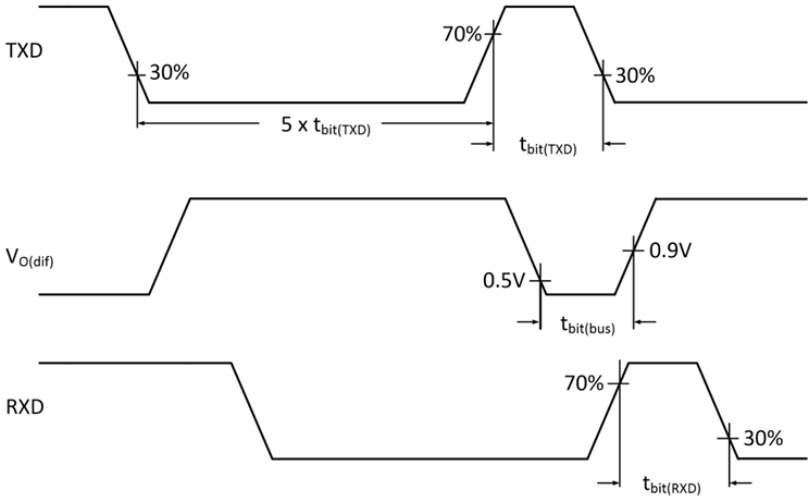
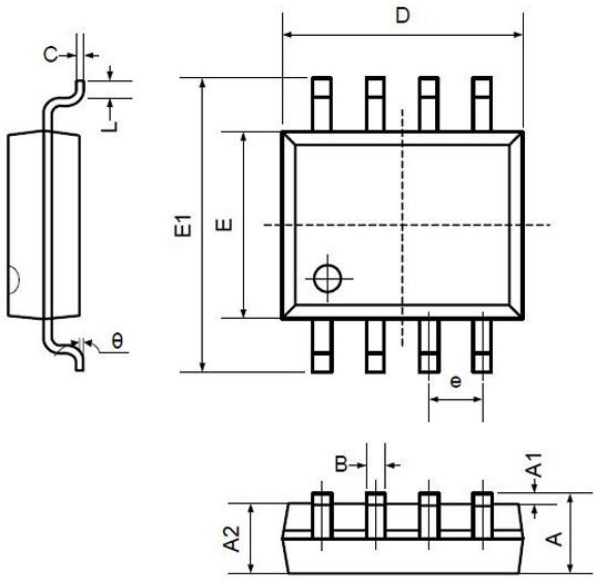


Fig 6. CAN FD Timing Definition According to ISO11898-2



PACKAGE INFORMATION

Dimension in SOP8 (Unit: mm)



Symbol	Min.	Max.
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
B	0.330	0.510
C	0.190	0.250
D	4.780	5.000
E	3.800	4.000
E1	5.800	6.300
e	1.270 TYP.	
L	0.400	1.270
θ	0°	8°

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