

**DESCRIPTION**

The AM016NS06HPJ is available in PDFN8(5x6) Package.

VDSS	RDS(ON) TYP.	ID
60V	1.6mΩ	200A

APPLICATIONS

- Battery management
- Synchronous Rectification in SMPS
- UPS

ORDERING INFORMATION

Package Type	Part Number	
PDFN8(5x6) SPQ: 5,000pcs/Reel	PJ8	AM016NS06HPJ8R
Note	R: Tape & Reel	
AiT provides all RoHS products		

ABSOLUTE MAXIMUM RATINGS

T_C = 25°C, unless otherwise specified.

VDSS, Drain-to-Source Voltage ⁽¹⁾		60V
VGSS, Gate-to-Source Voltage		±20V
ID, Continuous Drain Current	T _C = 25°C ⁽³⁾	200A
	T _C = 100°C	138A
IDM, Pulsed Drain Current at VGS=10V ⁽²⁾		780A
EAS, Single Pulsed Avalanche Energy, L=1mH		800mJ
PD, Power Dissipation T _C = 25°C		208W
PD, Derating Factor above T _A =25°C		1.7W/°C
RθJC, Thermal Resistance, Junction-to-Case		0.6°C/W
RθJA, Thermal Resistance, Junction-to-Ambient		50°C/W
TSTG, Storage Temperature Range		-55°C ~ +150°C
TJ, Junction Temperature Range		-55°C ~ +150°C
TL, Maximum Temperature for Soldering		300°C
TPAK, Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds,		260°C

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

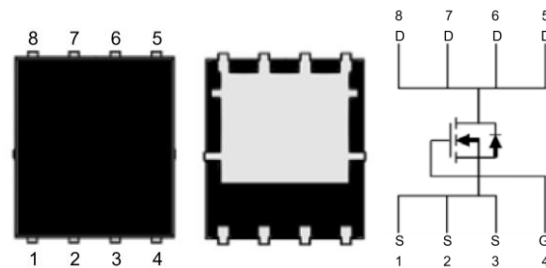
(1) T_J=+25°C to +150°C.

(2) Repetitive rating; pulse width limited by maximum junction temperature.

(3) Silicon limited current only.

FEATURE

- 60V, 200A
- RDS(ON) Typ.=1.6mΩ @ VGS =10V
- Proprietary New Trench Technology
- Fast Switching and High Efficiency
- Low On-Resistance

PIN DESCRIPTION

Pin #	Symbol	Function
1, 2, 3	S	Source
4	G	Gate
5,6,7,8	D	Drain



ELECTRICAL CHARACTERISTICS

T_J = 25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Off Characteristics						
Drain-to-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D = 250μA	60	-	-	V
Drain-to-Source Leakage Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
		V _{DS} =48V, V _{GS} =0V, T _J =125°C			100	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} = +20V, V _{DS} =0V	-	-	+100	nA
		V _{GS} = -20V, V _{DS} =0V	-	-	-100	
On Characteristics						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.00	-	4.00	V
Static Drain-Source ON-Resistance *	R _{DS(ON)}	V _{GS} = 10V, I _D = 30A	-	1.60	1.95	mΩ
Dynamic Characteristics						
Input Capacitance	C _{iss}	V _{DS} = 30V, V _{GS} =0V, f=1.0MHz	-	5092	-	pF
Output Capacitance	C _{oss}		-	2347	-	
Reverse Transfer Capacitance	C _{rss}		-	90	-	
Total Gate Charge	Q _g	V _{DD} = 30V , I _D =20A V _{GS} =10V	-	76	-	nC
Gate-Source Charge	Q _{gs}		-	20.6	-	
Gate-Drain(“Miller”) Charge	Q _{gd}		-	18.5	-	
Resistive Switching Characteristics						
Turn-On Delay Time	t _{d(on)}	V _{DD} =30V, I _D = 20A R _G =4.7Ω, V _{GS} = 10V	-	32.8	-	ns
Rise Time	t _r		-	20.2	-	
Turn-Off Delay Time	t _{d(off)}		-	58	-	
Fall Time	t _f		-	26	-	
Drain-Source Diode Characteristics						
Continuous Source Current	I _{SD}	Integral PN-diode in MOSFET	-	-	200	A
Pulsed Source Current	I _{SM}		-	-	780	A
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S = 80A	-	-	1.20	V
Reverse Recovery Time	t _{rr}	I _F = 80A, V _{GS} =0V	-	85	-	ns
Reverse Recovery Charge	Q _{rr}	di/dt=100A/us	-	60	-	nC

* Pulse Width≤380μs, Duty Cycle≤2%.



TYPICAL PERFORMANCE CHARACTERISTICS

Fig 1. On-Region Characteristics

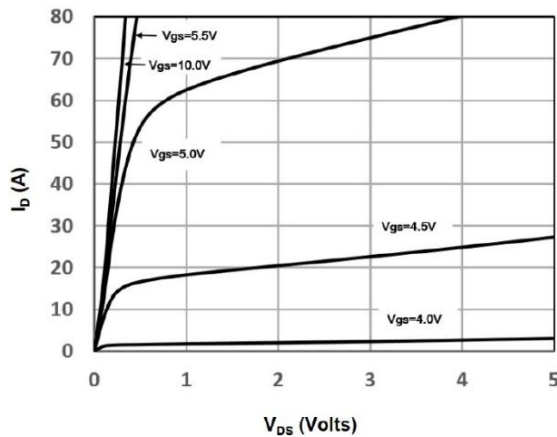


Fig 2. Transfer Characteristics

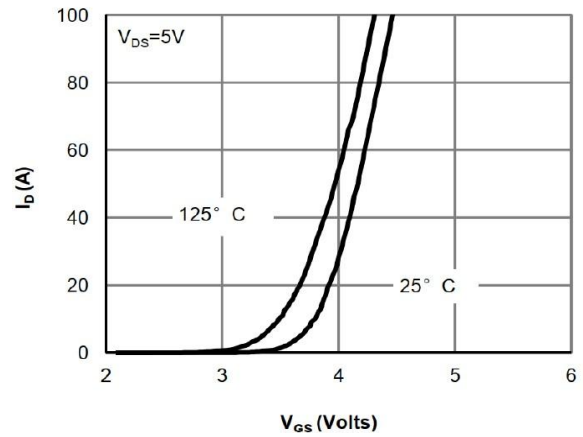


Fig 3. On-Resistance vs. Drain Current and Gate Voltage

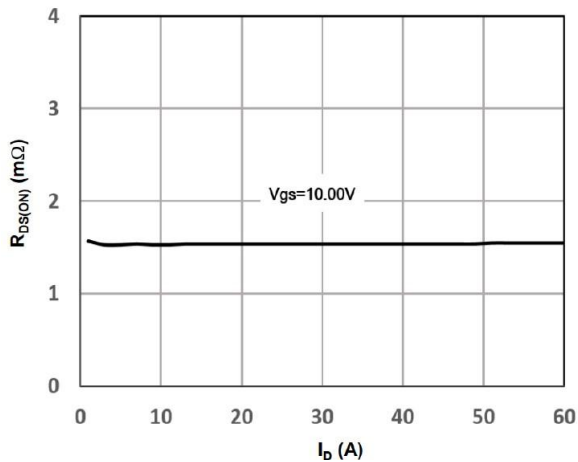


Fig 4. On-Resistance vs. Junction Temperature

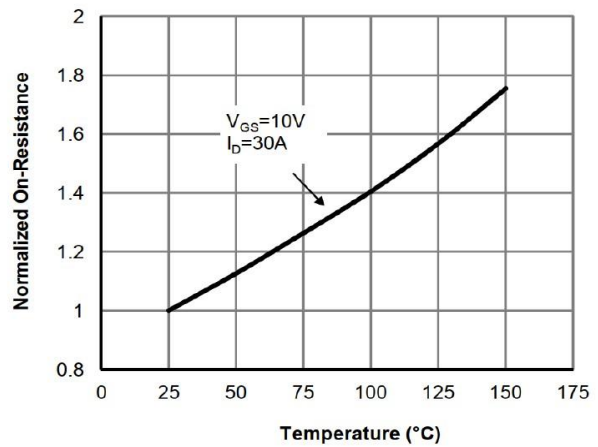


Fig 5. On-Resistance vs. Gate-Source Voltage

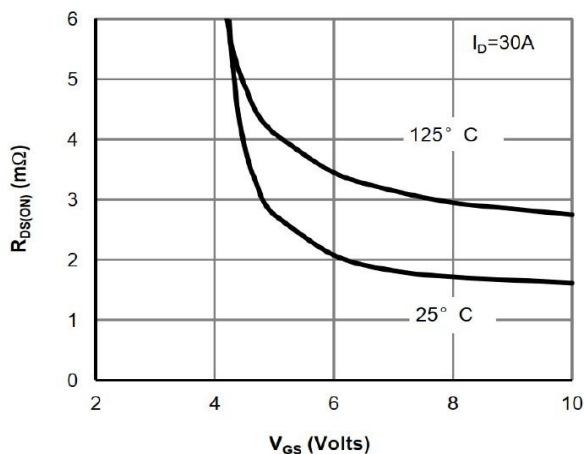


Fig 6. Body-Diode Characteristics

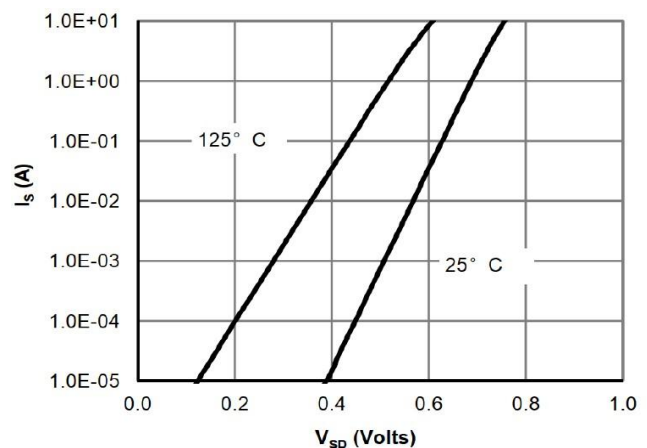




Fig 7. Gate-Charge Characteristics

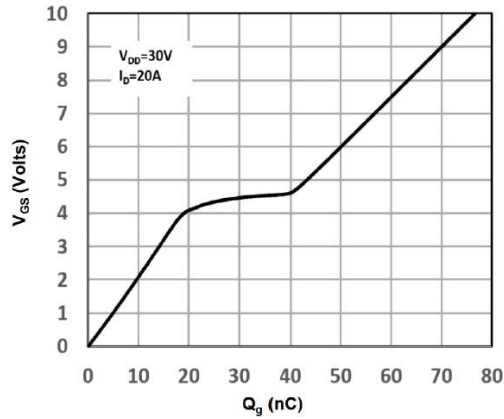


Fig 8. Capacitance Characteristics

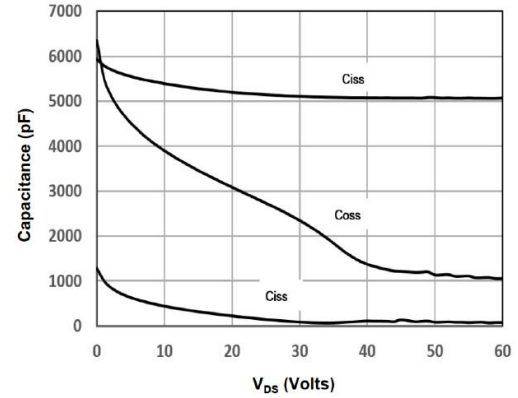
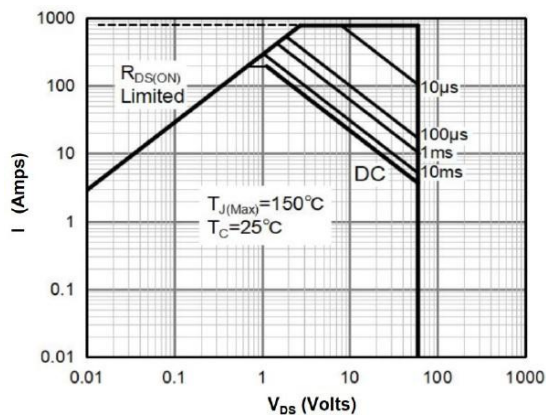


Fig 9. Maximum Forward Biased Safe Operating Area





TEST CIRCUITS AND WAVEFORMS

Fig 10. Peak Diode Recovery dv/dt Test Circuit

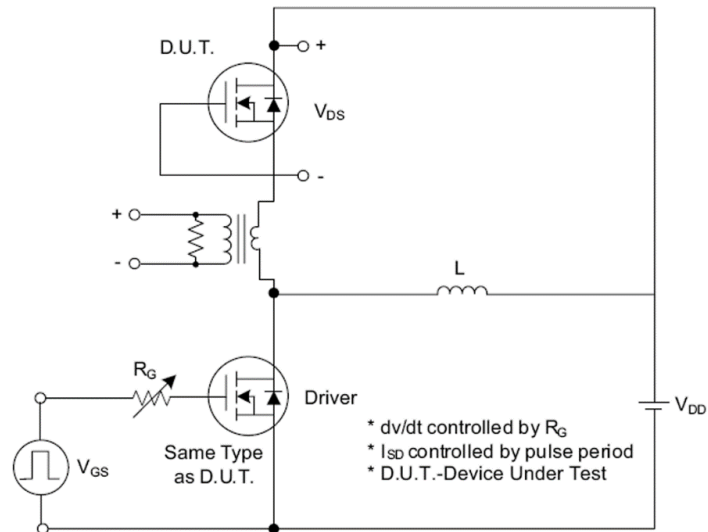


Fig 11. Peak Diode Recovery dv/dt Waveforms

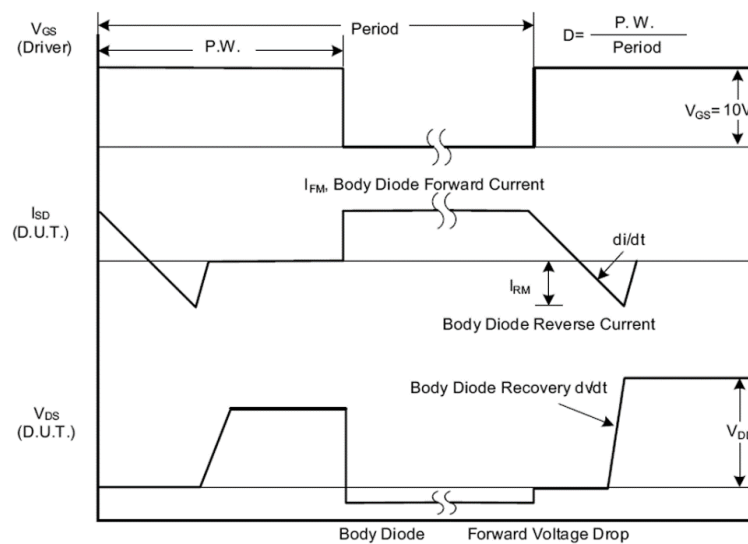




Fig 12. Switching Teat Circuit

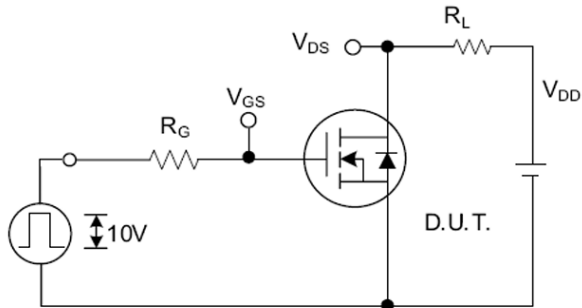


Fig 13. Switching Waveforms

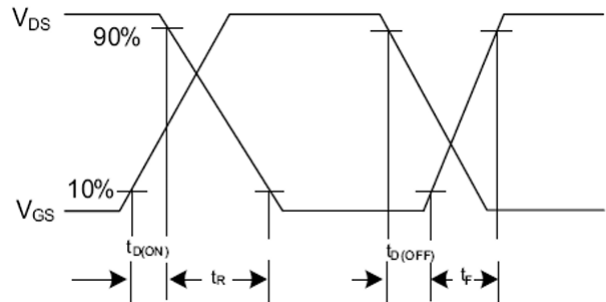


Fig 14. Gate Charge Test Circuit

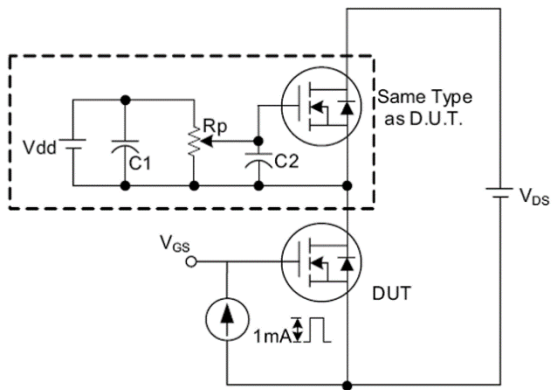


Fig 15. Gate Charge Waveform

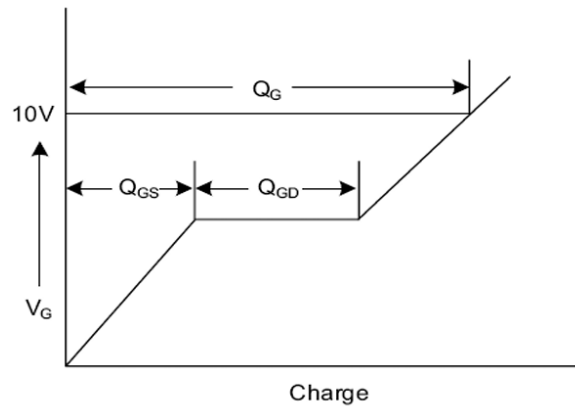


Fig 16. Unclamped Inductive Switching Teat Circuit

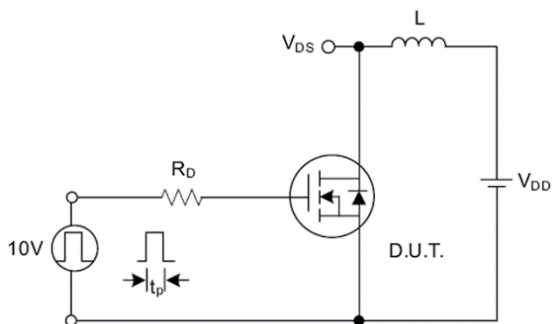
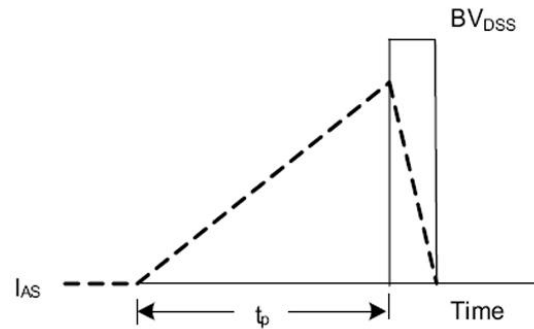


Fig 17. Unclamped Inductive Switching Waveform







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