DESCRIPTION

The AD8837 of devices provides an integrated motor driver solution for cameras, consumer products, toys, and other low-voltage or battery-powered motion control applications. The device can drive one dc motor or other devices like solenoids. The output driver block consists of N-channel power MOSFETs, Stop, Forward, Reverse and Brake Functions.

The AD8837 of devices can supply 1.8 A of maximum output current, 3.5A of peak current. It operates on a motor power supply voltage from 0 to 11V, and a device power supply voltage of 1.8V to 7V.

The AD8837 device has a PWM (IN1-IN2) input interface.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature.

The AD8837 is available DFN8 (2x2) package.

FEATURES

- H-Bridge Motor Driver
  - – Drives a DC Motor or Other Loads
  - – Low MOSFET On-Resistance: HS + LS 330 mΩ
- 1.8A Maximum Drive Current, 3.5A Peak Current
- Separate Motor and Logic Supply Pins:
  - – Motor V_M: 0 to 11V
  - – Logic V_{CC}: 1.8 to 7 V
- PWM or PH-EN Interface
  - – PWM, IN1 and IN2
- Low Iq: typ. 120 nA
- Protection Features
  - – V_{CC} Undervoltage Lockout (UVLO)
  - – Overcurrent Protection (OCP)
  - – Thermal Shutdown (TSD)
- Available in DFN8 (2x2) package

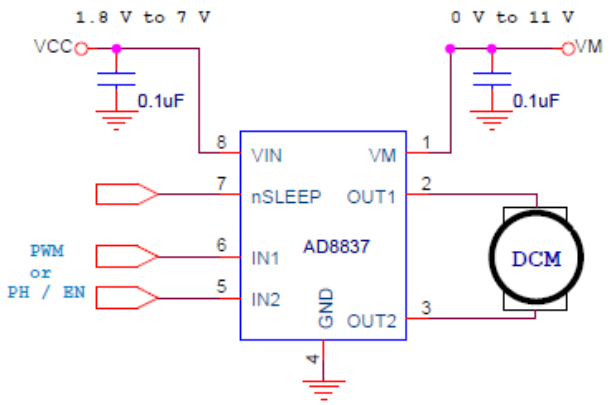
APPLICATION

- Cameras
- DSLR Lenses
- Consumer Products
- Toys
- Robotics
- Medical Devices

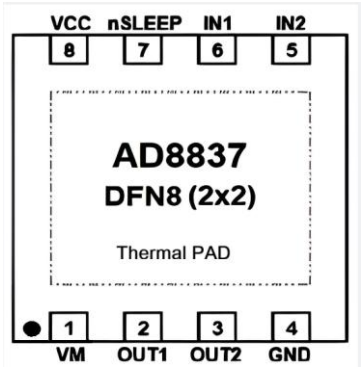
ORDERING INFORMATION

Package Type	Part Number	
DFN8(2x2) SPQ: 3,000pcs/Reel	J8	AD8837J8R
		AD8837J8VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

TYPICAL APPLICATION



PIN DESCRIPTION



DFN8(2x2), J8

Top View

Pin # DFN8(2x2)	Symbol	Type	Function
1	V_M	PWR	Motor Supply Voltage Bypass this pin to the GND with a 0.1μF ceramic capacitor.
2	OUT1	O	Motor Output 1 Connect these pins to the motor winding.
3	OUT2	O	Motor Output 2 Connect these pins to the motor winding.
4	GND	PWR	Device ground. This pin must be connected to ground
5	IN2	I	Input logic 2
6	IN1	I	Input logic 1
7	nSLEEP	I	The Sleep mode pin includes an internal pull-down resistor. A logic Low on this pin forces the device into low-power Sleep mode, while a logic High allows the device to operate in normal mode.
8	V_{CC}	PWR	Logic power supply Bypass this pin to the GND with a 0.1μF ceramic capacitor.
-	Thermal PAD	PWR	Exposed pad (heatsink) - connects to ground for proper thermal dissipation.

ABSOLUTE MAXIMUM RATINGS

V_M, Motor Power-Supply Voltage	-0.3V ~ 12V
Vcc, Logic Power Supply Voltage	-0.3V ~ 7V
V_{IN}, IN1, IN2 Input Logic Voltage	-0.5V ~7V
I_{OUT}, OUT1, OUT2 Peak Drive Current	Internally Limited
T_J, Junction Temperature	-40°C ~ +150°C
T_A, Environment Temperature	-40°C ~ +85°C
T_{STG}, Storage Temperature	-55°C ~ +150°C
T_L, Lead Pin Temperature	+300°C

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

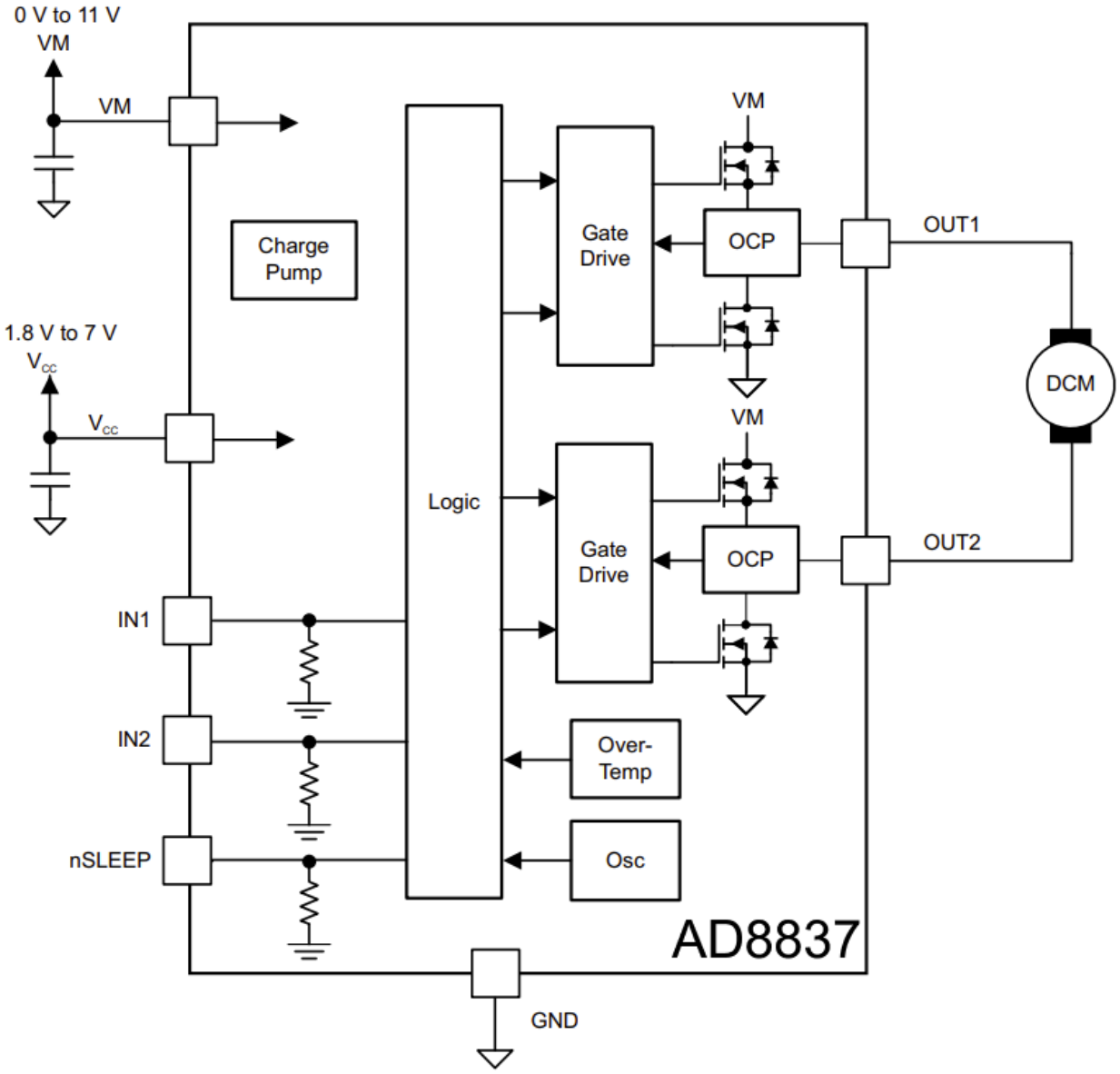
ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{BB} = 24V , C_L=1nF ,unless otherwise specified.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
REGULAR PARAMETERS						
Logic Power Supply Voltage	V_{CC}		1.8	-	7	V
Motor Power Supply Voltage	V_M		0	-	11	V
V_M Operating Current	I_{VM}	V_M=5V, V_{CC}=3V, f_{PWM} = 0	-	50	100	μA
		V_M=5V, V_{CC}=3V, f_{PWM} = 50 kHz	-	0.3	1.2	mA
V_M Quiescent Current	I_{VM-Q}	V_M=5V, V_{CC}=3V, nSLEEP = 0	-	30	95	nA
V_{CC} Operating Current	I_{CC}	V_M=5V, V_{CC}=3V, f_{PWM} = 0	-	250	450	μA
		V_M=5V, V_{CC}=3V, f_{PWM} = 50 kHz	-	0.35	1.20	mA
V_{CC} Quiescent Current	I_{CC-Q}	V_M=5V, V_{CC}=3V, nSLEEP = 0	-	5	25	nA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
MOTOR DRIVER OUTPUT						
HS + LS FET On-Resistance	$R_{DS(ON)}$	I_{OUT}=800mA, V_M=5, V_{CC}=3V, T_J=25°C	-	0.33	0.38	Ω
Off-State Leakage Current	I_{OFF}	V_{OUT}=0	-200	-	200	nA
CONTROL INPUTS (IN1/IN2)						
High Level Input Voltage	V_{INH}		-	0.46xV_{CC}	0.5xV_{CC}	V
Low Level Input Voltage	V_{INL}		0.25xV_{CC}	0.38xV_{CC}	-	
Logic Input Hysteresis	V_{HYS}		-	0.08xV_{CC}	-	
High Level Input Current	I_{INH}	V_{IN}=3.3V	-	-	50	μA
Low Level Input Current	I_{INL}	V_{IN}=0V	-5	-	5	
Pulldown Resistance	R_{PD}		-	100	-	KΩ
		nSLEEP	-	55	-	
PROTECTION CIRCUITS						
Vcc Undervoltage Lockout	V_{UVLO_R}	V_{BB} Increasing	-	-	1.7	V
Vcc Undervoltage Lockout Hysteresis	V_{UVLO_HYS}		-	0.1	-	mV
Overcurrent Protection Trip Level	I_{OCP}		1.9	-	3.5	A
Overcurrent Protection Filter Burr Time	t_{DEG}		-	1	-	μs
Overcurrent Retry Time	t_{RETRY}		-	1	-	ms
Thermal Shutdown Temperature	T_{TSD}	Temperature increasing	150	160	180	°C
Thermal Shutdown Hysteresis	$T_{TSD-HYS}$	Recovery = $T_{JTSD} - T_{TSDhys}$	-	15	-	°C

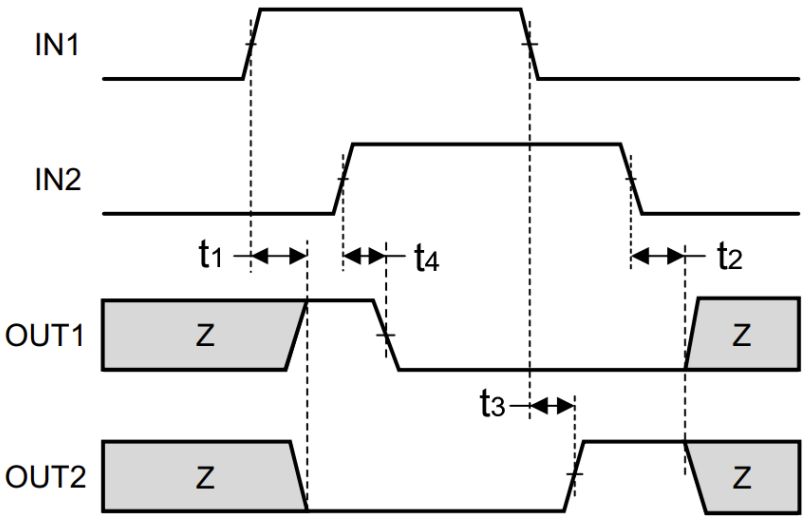
BLOCK DIAGRAM

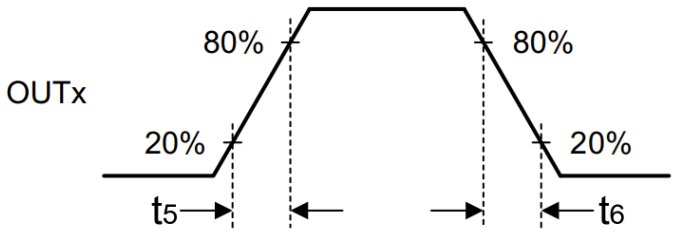


TIMING REQUIREMENTS

V_{CC}=3V, V_M=5V, T_A=25°C, R_{LOAD}=20Ω

Time	Parameter	Max	Unit
t_1	Output enable time	300	ns
t_2	Output disable time	300	ns
t_3	Delay time, INx high to OUTx high	160	ns
t_4	Delay time, INx low to OUTx low	160	ns
t_5	Output rise time	30 ~ 188	ns
t_6	Output fall time	30 ~ 188	ns
	Wake-up Delay, Time from nSLEEP rising edge to IC normal operation	30	μs

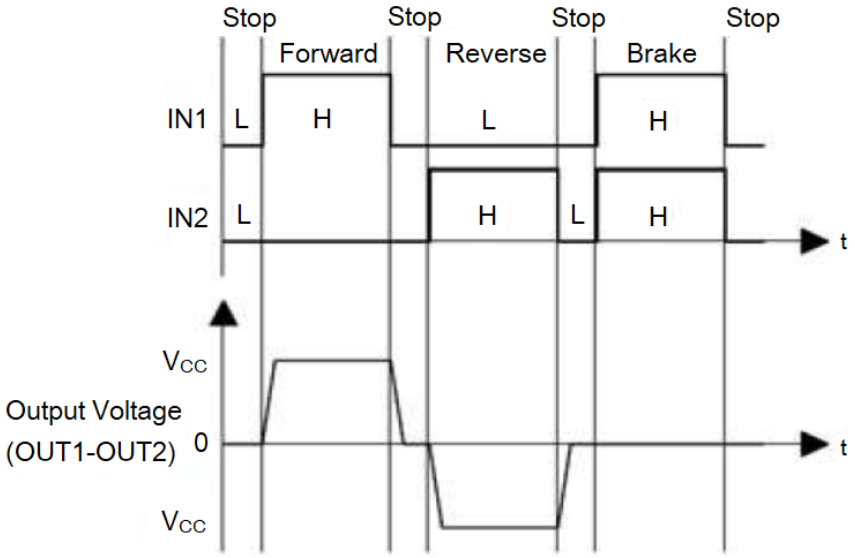




INPUT-OUTPUT LOGIC TABLE

nSLEEP	IN1	IN2	OUT1	OUT2	Function
L	X	X	Hi-Z	Hi-Z	Coasting
H	L	L	Hi-Z	Hi-Z	Coasting
H	L	H	L	H	Reverse
H	H	L	H	L	Forward
H	H	H	L	L	Brake (Slow Decay Operation)

INPUT-OUTPUT WAVEFORM



Function Description

Overview

The AD8837 is an H-bridge driver capable of driving a DC motor or other devices such as solenoids. The outputs are controlled via the PWM inputs IN1 and IN2.

The device features a low-power Sleep mode, which can be enabled using the nSLEEP pin.

The AD8837 integrates both the FET drivers and the FET control circuitry, significantly reducing the number of external components required for a motor driver system. In addition, the device includes several protection features, such as undervoltage lockout (UVLO), overcurrent protection (OCP), and thermal shutdown (TSD).

Low-Power Sleep Mode

When the nSLEEP pin is driven Low, the AD8837 enters a low-power Sleep mode. In this state, all non-essential internal circuits are disabled, minimizing power consumption.

Power and Input Pins

- The input pins can be driven within the recommended operating range regardless of the presence of V_{CC} or V_M. No leakage paths exist when the power supply is absent.
- Each input pin includes a weak internal pull-down resistor (~100 kΩ) to GND.
- V_{CC} and V_M can be powered on or off in any sequence.
    - When V_{CC} is turned off, the device enters a low-power state and draws minimal current from V_M.
    - Logic supply voltage can range from 1.8V to 7V; in this case, V_{CC} and V_M can be tied together.
- V_M does not have undervoltage lockout (UVLO); as long as V_{CC} > 1.8V, the internal logic remains active.
- V_M voltage may drop to 0 V, but the load may not be fully driven at low V_M voltage.

V_{CC} Undervoltage Lockout (UVLO)

- If V_{CC} falls below the UVLO threshold, all FETs in the H-bridge are disabled.
- Normal operation resumes once V_{CC} rises above the UVLO threshold.

Overcurrent Protection (OCP)

- Each FET includes an analog current limit circuit that restricts current by disabling the gate driver.
- If the analog current limit persists beyond t_{DEG} (~1 µs), all H-bridge FETs are disabled and automatically recover after a delay t_{OCP}.
- Overcurrent is detected on both high-side and low-side FETs.
- Conditions triggering overcurrent protection include:
  - Short to V_M or GND
  - Short from OUT1 to OUT2

Thermal Shutdown (TSD)

- If the junction temperature (TJ) exceeds the safe limit, all FETs in the H-bridge are disabled.
- Normal operation automatically resumes when the temperature drops back to a safe level.

Fault Conditions Summary

Fault Condition	Trigger Condition	H-Bridge State	Recovery Condition
V_{CC} Undervoltage (UVLO)	V_{CC} < 1.7V	All FETs off	V_{CC}>1.8V
Overcurrent Protection (OCP)	I_{OUT} > 1.9 A (min)	All FETs off	After t_{RETRY}
Thermal Shutdown (TSD)	T_J > 150℃ (min)	All FETs off	T_J > 140℃

Device Operating Modes

- Normal Operation: Unless the nSLEEP pin is driven Low, the AD8837 operates in normal mode.
- Sleep Mode: When nSLEEP = Low, the device enters low-power Sleep mode, and all H-bridge FETs are disabled (Hi-Z state). When nSLEEP is driven High, the device automatically exits Sleep mode.
- Fault Mode: During UVLO (V_{CC} undervoltage), OCP (overcurrent), or TSD (thermal shutdown) events, the H-bridge outputs are disabled. Normal operation resumes once the fault condition is cleared.

Operating Mode	Condition	H-Bridge State	Notes
Normal Operation	nSLEEP = High	Driving	—
Sleep Mode	nSLEEP = Low	All FETs off	H-bridge outputs in Hi-Z
Fault Mode	UVLO, OCP, TSD	All FETs off	Outputs remain off until the fault is cleared

Typical Operating Conditions

Parameter	Symbol	Example Value	Unit
Motor Supply Voltage	V_M	9	V
Logic Supply Voltage	V_{CC}	3.3	V
Output Drive Current	I_{OUT}	800	mA

Device Power Dissipation

The power dissipation of the AD8837 is primarily determined by the on-resistance of the output FETs ($R_{DS(ON)}$). The approximate average power dissipation during motor operation can be calculated as:

$$P_{TOT}=R_{DS(ON)}\times(I_{OUT(RMS)})^2$$

Where:

- P_{TOT} = Total power dissipation of the device
- $R_{DS(ON)}$ = Sum of the on-resistances of the high-side and low-side FETs
- $I_{OUT(RMS)}$ = RMS or DC current delivered to the load.

The maximum allowable power dissipation depends on the ambient temperature and thermal management. Note that $R_{DS(ON)}$ increases with temperature, so device power dissipation rises as the chip heats up.

The AD8837 features thermal shutdown protection (TSD). If the junction temperature exceeds approximately 150°C, the H-bridge FETs are disabled until the temperature drops back to a safe level. Thermal shutdown indicates excessive power dissipation, insufficient cooling, or high ambient temperature.

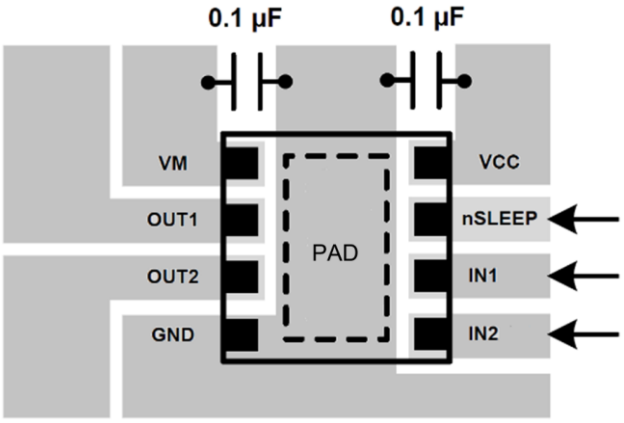
Recommended Operating Power Supply

- Power-On Sequence:
  V_{CC} and V_M can be powered on or off in any sequence. When V_{CC} is turned off, the device enters a low-power state, drawing minimal current from V_M.
- Logic Supply Voltage:
  When the logic supply voltage is between 1.8 V and 7 V, V_{CC} and V_M can be connected together.
- Bypass Capacitors:
  Connect 0.1 µF ceramic capacitors from V_M and V_{CC} to GND. Place these capacitors as close as possible to the V_M and V_{CC} pins.
- V_M Undervoltage Note:
  The V_M supply does not have undervoltage lockout (UVLO); as long as V_{CC} > 1.8 V, the internal logic remains active.

Note: V_M may drop to 0 V under certain conditions, but the load may not be fully driven if V_M voltage is too low.

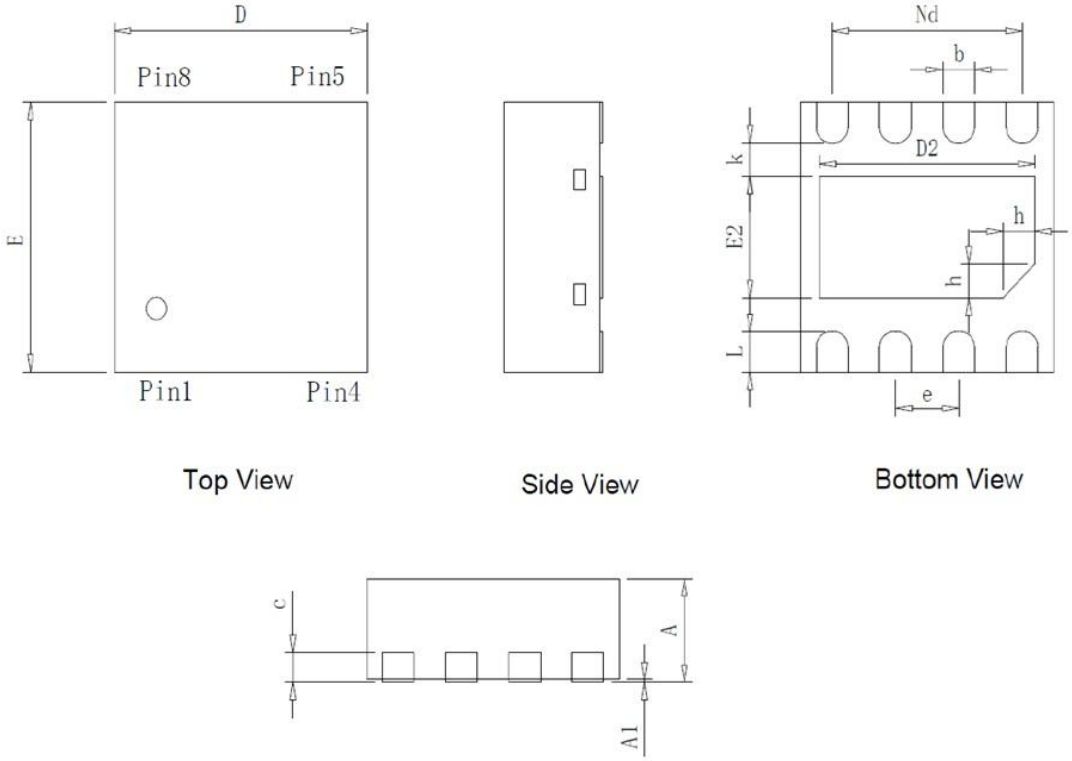
Layout Guidelines

- Bypass Capacitors: Use low-impedance ceramic capacitors (recommended 0.1 μF) between V_M/V_{CC} and GND.
- Placement: Place these capacitors as close as possible to the V_M and V_{CC} pins.
- Grounding: Connect the capacitors to the device GND pin using wide traces or a ground plane to ensure proper decoupling and minimize voltage drops.



PACKAGE INFORMATION

Dimension in DFN8(2x2) (Unit: mm)



Symbol	Min	Max
A	0.700	0.800
A1	0.000	0.050
b	0.200	0.300
c	0.203REF	
D	1.900	2.100
D2	1.600	1.800
Nd	1.500 BSC	
e	0.500 BSC	
E	1.900	2.100
E2	0.800	1.000
h	0.200	0.300
k	0.200	0.300
L	0.250	0.350

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