DESCRIPTION

The A93C46 (1K Bit) is Electrically Erasable Programmable Memory (EEPROM) devices accessed through the MICROWIRE™ bus protocol. The memory arrays can be configured either in bytes (x8b) or in words (x16b).

The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation is essential.

The A93C46 is available in SOP8, SSOP8, TSSOP8 and DFN8 Packages.

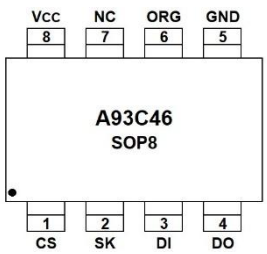
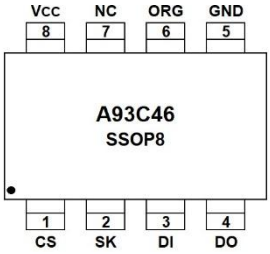
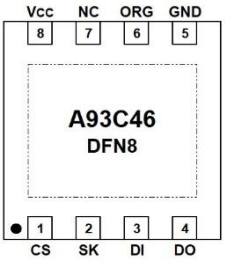
FEATURES

- Industry Standard MICROWIRE™ Bus
- Low-Voltage Operation: V_{CC} = 1.7V to 5.5V
- Dual Organization: by word (x16) or byte (x8)
- Programming Instructions Byte, Word or Entire Memory
- Sequential Read Operation.
- 2 MHz Clock Rate (5V)
- Self-Timed Write Cycle within 3ms Maximum.
- High Reliability:
  Endurance: 4,000,000 Write Cycles
  Data Retention: 100 Years
- Available in SOP8, SSOP8, TSSOP8 and DFN8 Packages

ORDERING INFORMATION

Package Type	Part Number		
SOP8 SPQ:2,500pcs/Reel	M8	A93C46M8R-A	A93C46M8VR-A
			A93C46M8VR-B
			A93C46M8VR-C
SSOP8 SPQ:3,000pcs/Reel	MX8	A93C46MX8R-A	A93C46MX8VR-A
			A93C46MX8VR-B
			A93C46MX8VR-C
TSSOP8 SPQ: 3,000pcs/Reel	TMX8	A93C46TMX8R-A	A93C46TMX8VR-A
			A93C46TMX8VR-B
			A93C46TMX8VR-C
DFN8 SPQ: 3,000pcs/Reel	J8	A93C46J8R-A	A93C46J8VR-A
			A93C46J8VR-B
			A93C46J8VR-C
Note	Temperature: A : -40℃ to +85℃ B : -40℃ to +105℃ C : -40℃ to +125℃: V :Halogen Free Package R : Tape & Reel		
AiT provides all RoHS products			

PIN DESCIPTION

			
SOP8, M8 Top View	SSOP8, MX8 Top View	TSSOP8, TMX8 Top View	DFN8, J8 Top View

Pin # SOP8 / SSOP8 / TSSOP8 / DFN8	Symbol	Type	Functions
1	CS	I	Chip Select
2	SK	I	Serial Data Clock
3	DI	I	Serial Data Input
4	DO	O	Serial Data Output
5	GND	-	Ground
6	ORG	I	Organization Select
7	NC	-	Not Connect
8	V_{CC}	-	Power Supply

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	-40℃ ~ +130℃
Storage Temperature	-65℃ ~ +150℃
DC Supply Voltage	-0.3V ~ 6.5V
Input / Output Voltage	-0.3V ~ V_{CC} +0.3V
Electrostatic Pulse (HBM)	4000V
Electrostatic Pulse (MM)	250V
Electrostatic Pulse (CDM)	2000V

Stresses above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RELIABILITY CHARACTERISTICS

Applicable over recommended operating range from T_A = 25℃, f = 1.0 MHz, V_{CC} = +5.0V

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$	-	-	8	pF
Input Capacitance	C_{IN}	-	-	6	pF

DC ELECTRICAL CHARACTERISTICS

T_A = 25℃, f = 1.0 MHz, V_{CC} = +5.0V, unless otherwise specified.

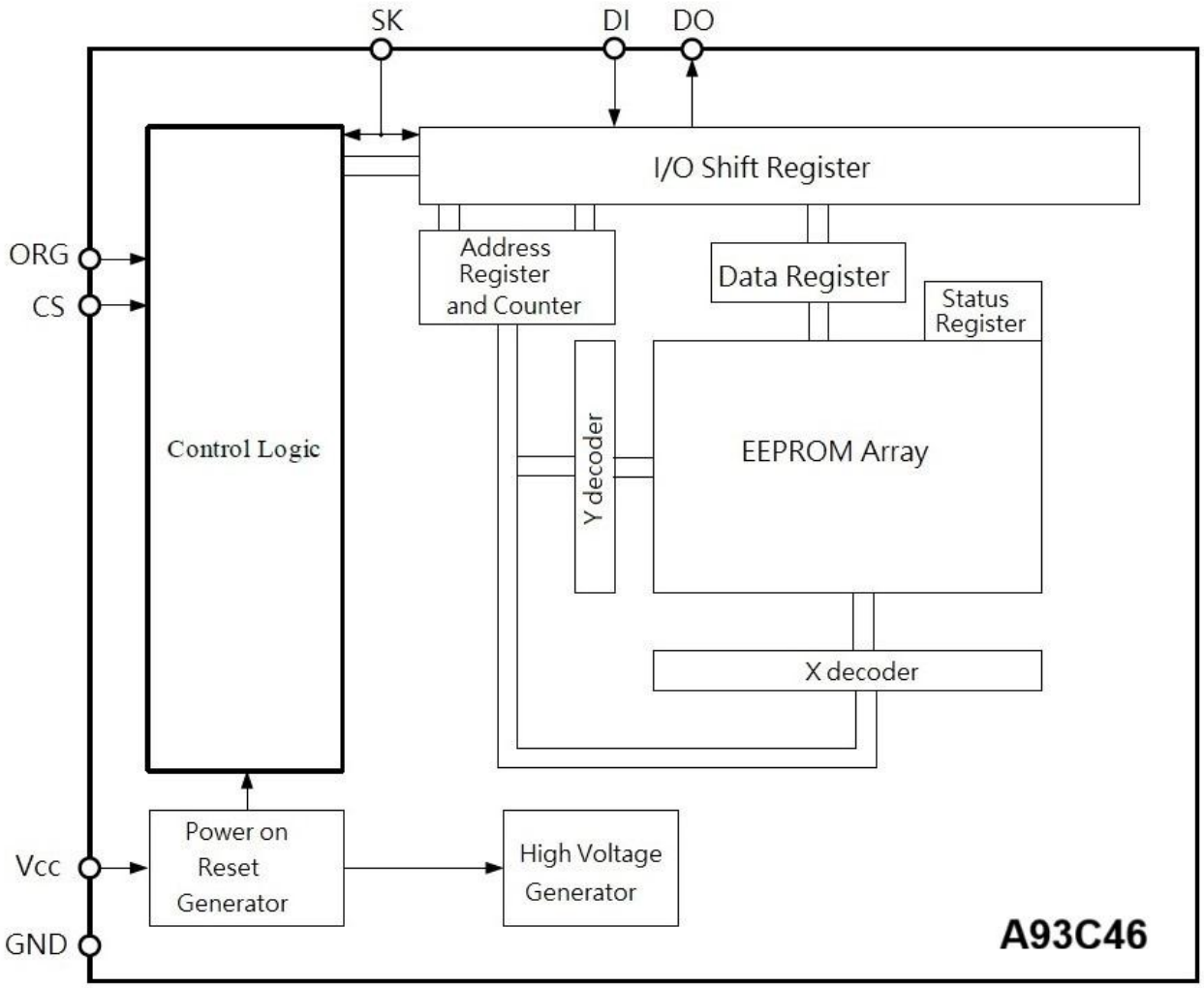
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	-	1.8	-	5.5	V
Input Leakage Current	I_{LI}	-	-	-	±2.5	μA
Output Leakage Current	I_{LO}	-	-	-	±2.5	μA
Operating Supply Current (Read)	$I_{CC\text{-}Read}$	-	-	0.5	2.0	mA
Operating Supply Current (Write)	$I_{CC\text{-}Write}$	-	-	2.0	3.0	mA
Standby Supply Current	I_{SB2}^*	-	-	0.1	5.0	μA
Input Low Level	V_{IL}	-	-0.3	-	V_{CC} x 0.3	V
Input High Level	V_{IH}	-	V_{CC} x 0.7	-	V_{CC} + 0.3	V
Output Low Level	V_{OH}	-	-	-	0.2	V
Output High Level	V_{OH}	-	V_{CC} x 0.7	-	-	V

AC ELECTRICAL CHARACTERISTICS

T_A = 25℃, f = 1.0 MHz, V_{CC} = +5.0V, unless otherwise specified.

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock Frequency	f_{SK}	-	DC	-	2	MHz
Chip Select Low to Clock High	-	-	50	-	-	ns
Chip Select Setup Time	t_{CSS}	-	50	-	-	ns
Chip Select Low to Chip Select High	t_{CS}	-	200	-	-	ns
Clock High Time	t_{SKH}	-	200	-	-	ns
Clock Low Time	t_{SKL}	-	200	-	-	ns
Data In Setup Time	t_{DIS}	-	50	-	-	ns
Data In Hold Time	t_{DIH}	-	50	-	-	ns
Clock Setup Time (Relative To S)	t_{SKS}	-	50	-	-	ns
Chip Select Hold Time	t_{CSH}	-	0	-	-	ns
Chip Select to READ/$\overline{BUSY}$ Status	t_{SV}	-	-	-	200	ns
Chip Select Low to Output Hi-Z	t_{DF}	-	-	-	100	ns
Delay to Output Low	t_{PD0}	-	-	-	200	μs
Delay to Output Valid	t_{PD1}	-	-	-	200	ns
Erase or Write Cycle Time	t_{WP}	-	-	-	3	ms
Write Cycle Endurance		-	4M	-	-	Write Cycle

BLOCK DIAGRAM



DETAILED INFORMATION

Chip Select (CS): The Chip Select (CS) pin is used to control device selection. The A93C46 is selected when the CS pin is high. When the device is not selected, data will not be accepted via the Serial Data Input (DI) pin, and the Serial Output (DO) pin will remain in a high-impedance state.

Serial Data Clock (SK): The Serial Data Clock (SK) pin is used to synchronize the communication between a master and the A93C46. Instructions, addresses or data present on the Serial Data Input (DI) pin is latched in on the rising edge of SK, while output on the Serial Data Output (DO) pin is also clocked out on the rising edge of SK.

Serial Data Input (DI): The Serial Data Input (DI) pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the Serial Data Clock (SK).

Serial Data Output (DO): The Serial Data Output (DO) pin is used to transfer data out of the A93C46. During a read sequence, data is shifted out on this pin after the rising edge of the Serial Data Clock (SK). This pin also outputs the Ready/Busy status of the part if CS is brought high after being low for a minimum of tcs and an erase or write operation has been initiated.

Ground (GND): The ground reference for the power supply. The Ground (GND) pin should be connected to the system ground.

Internal Organization (ORG): The Internal Organization (ORG) pin is used to select between the x16 or x8 memory organizations of the device. When the ORG pin is tied to V_{CC}, the x16 memory organization is selected. When the ORG pin is tied to GND, the x8 memory organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1MΩ pull-up resistor, then the x16 organization is selected.

Device Power Supply (V_{CC}): The Device Power Supply (V_{CC}) pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.

FUNCTION DESCRIPTION

1. Memory Organization

The A93C46 is Electrically Erasable Programmable Memory (EEPROM) devices accessed through the MICROWIRE™ bus protocol. The memory array can be configured either in bytes (x8b) or in words (x16b).

The A93C46 memory is organized either as bytes (x8) or as words (x16). If Organization Select (ORG) is unconnected (or connected to V_{CC}) the x16 organization is selected; when Organization Select (ORG) is connected to Ground the x8 organization is selected. When theA93C46 is in Standby mode, Organization Select (ORG) should be set either to GND or V_{CC} to reach the device minimum power consumption (as any voltage between GND and V_{CC} applied to ORG input may increase the device Standby current).

Table 1

Device	Number of Bits	Number of 8-Bits Bytes	Number of 8-Bits Words
A93C46	1024	128	64

2. Instructions

The A93C46 is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the Host processor. A valid instruction starts with a rising edge of CS and consists of a Start bit (SB), followed by the appropriate opcode, and the desired memory address location.

Table 2

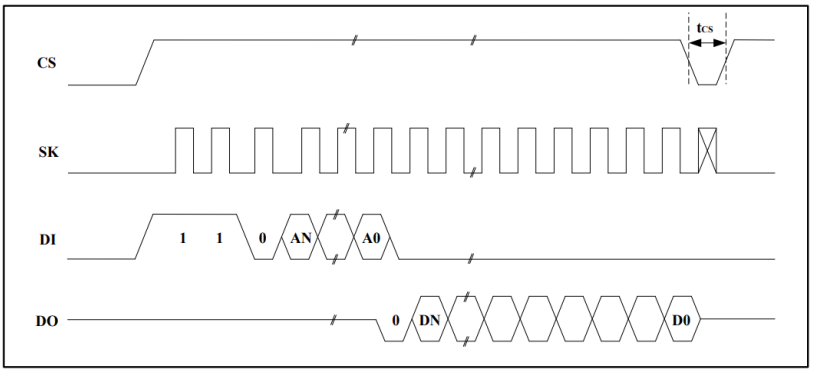
Instruction	Description	Start Bit	Op-Code	x8 Origination (ORG=0)		x16 Origination (ORG=1)	
				Address (1)	Data	Address (1)	Data
READ	Read Data from Memory	1	10	A6-A0	D7-D0	A5-A0	D15-D0
WRITE	Write Data from Memory	1	01	A6-A0	D7-D0	A5-A0	D15-D0
EWEN	Write Enable	1	00	11X XXXX	-	11 XXXX	-
EWDS	Write Disable	1	00	00X XXXX	-	00 XXXX	-
ERASE	Erase Byte or Word	1	11	A6-A0	-	A5-A0	-
ERAL	Erase all Memory	1	00	10X XXXX	-	10 XXXX	-
WRAL	Write all Memory with Same Data	1	00	01X XXXX	D7-D0	01 XXXX	D15-D0

(1) X = Don't Care bit

3. Read

The Read Data from Memory (READ) instruction outputs data on Serial Data Output (DO). When the instruction is received, the op-code and address are decoded, and the data from the memory is transferred to an output shift register. A dummy 0 bit is output first, followed by the 8-bit byte or 16-bit word, with the most significant bit first. Output data changes are triggered by the rising edge of Serial Clock (SK). The A93C46 automatically increments the internal address register and clocks out the next byte (or word) as long as the Chip Select Input (CS) is held High. In this case, the dummy 0 bit is not output between bytes (or words) and a continuous stream of data can be read (the address counter automatically rolls over to 00h when the highest address is reached).

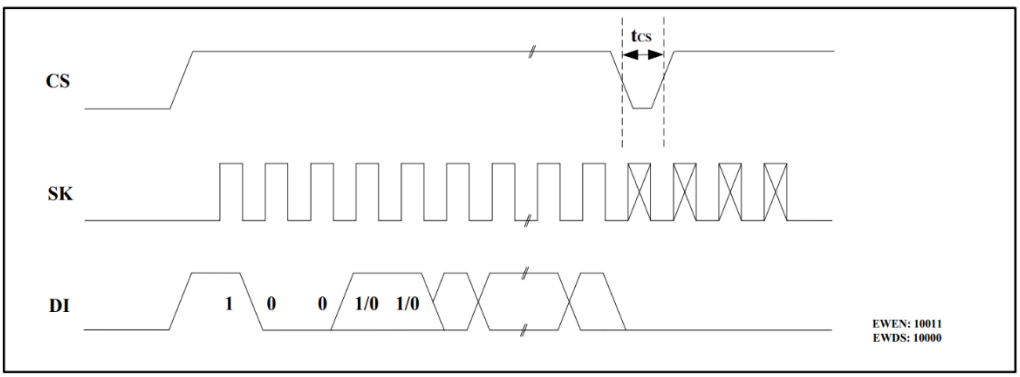
Fig 1.



4. Erase and Write Data

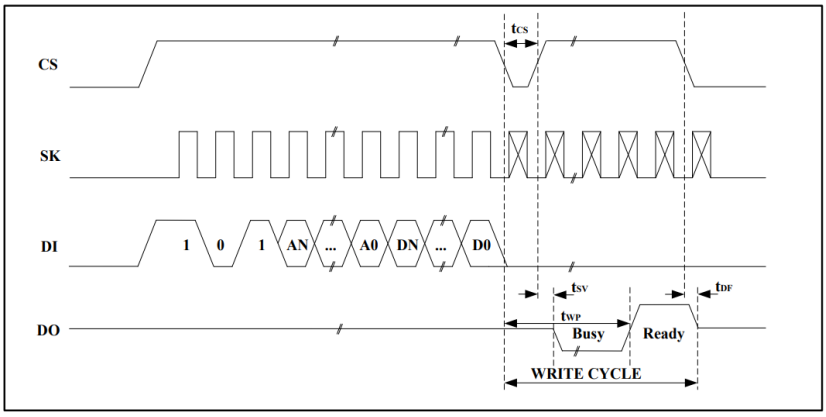
Write Enable and Write Disable: The Write Enable (EWEN) instruction enables the future execution of erase or write instructions, and the Write Disable (EWDS) instruction disables it. When power is first applied, the A93C46 initializes itself so that erase and write instructions are disabled. After a Write Enable (EWEN) instruction has been executed, erasing and writing remains enabled until a Write Disable (EWDS) instruction is executed, or until V_{CC} falls below the power-on reset threshold voltage. To protect the memory contents from accidental corruption, it is advisable to issue the Write Disable (EWDS) instruction after every write cycle. The Read Data from Memory (READ) instruction is not affected by the Write Enable (EWEN) or Write Disable (EWDS) instructions.

Fig 2.



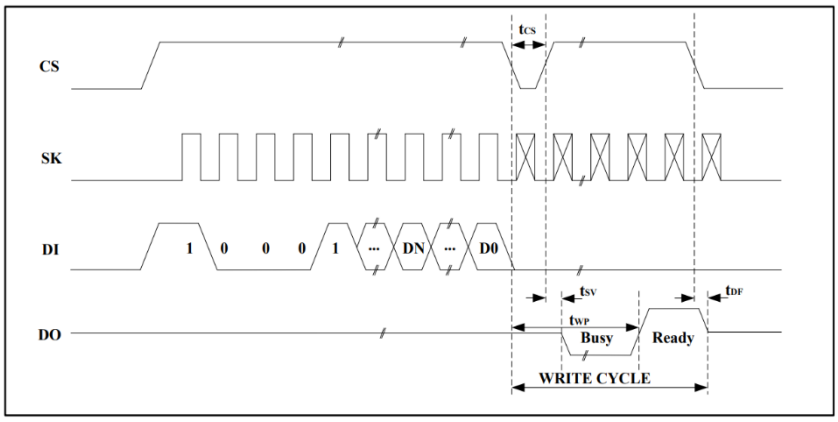
Write: For the Write Data to Memory (WRITE) instruction, 8 or 16 data bits follow the op-code and address bits. These form the byte or word that is to be written. As with the other bits, Serial Data Input (DI) is sampled on the rising edge of Serial Clock (SK). After the last data bit has been sampled, the Chip Select Input (CS) must be taken low before the next rising edge of Serial Clock (SK). If Chip Select Input (CS) is brought low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed. The completion of the cycle can be detected by monitoring the READY/BUSY line, as described later in this document. Once the Write cycle has been started, it is internally self-timed (the external clock signal on Serial Clock (SK) may be stopped or left running after the start of a Write cycle). The Write cycle is automatically preceded by an Erase cycle, so it is unnecessary to execute an explicit erase instruction before a Write Data to Memory (WRITE) instruction.

Fig 3.



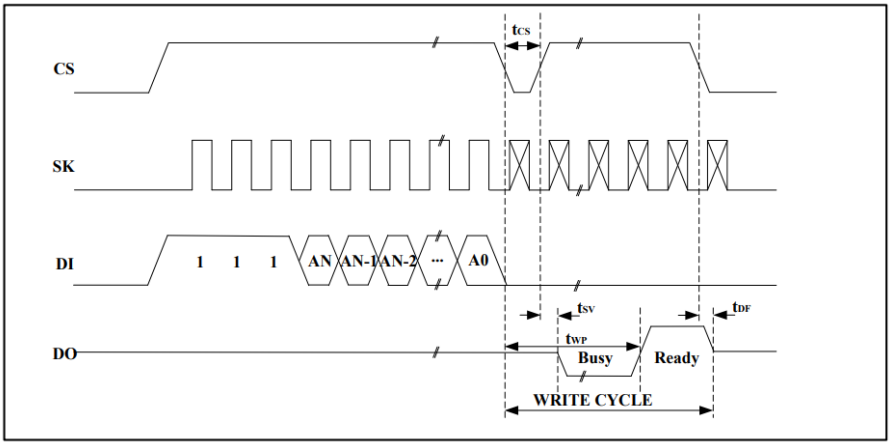
Write All: As with the Erase All Memory (ERAL) instruction, the format of the Write All Memory with same Data (WRAL) instruction requires that a dummy address be provided. As with the Write Data to Memory (WRITE) instruction, the format of the Write All Memory with same Data (WRAL) instruction requires that an 8-bit data byte, or 16-bit data word, be provided. When the ORG is valid, the two bytes of data should be the same. This value is written to all the addresses of the memory device. The completion of the cycle can be detected by monitoring the READY/BUSY line, as described next.

Fig 4.



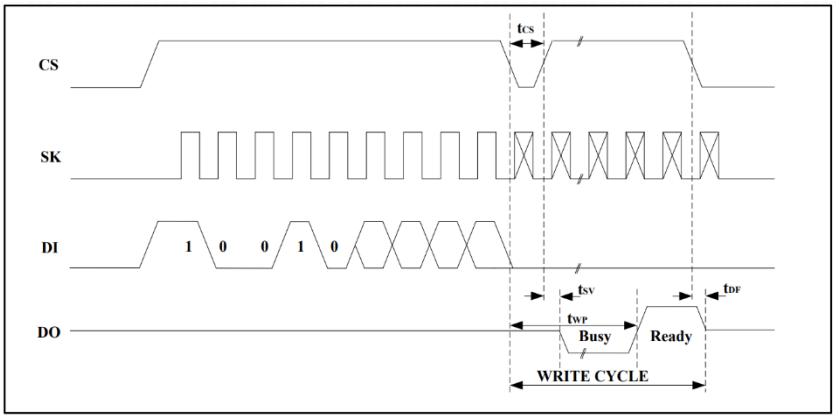
Erase Byte or Word: The Erase Byte or Word (ERASE) instruction sets the bits of the addressed memory byte (or word) to 1. Once the address has been correctly decoded, the falling edge of the Chip Select Input (CS) starts the self-timed Erase cycle. The completion of the cycle can be detected by monitoring the READY/BUSY line, as described in next Section: READY/BUSY status.

Fig 5.



Erase All: The Erase All Memory (ERAL) instruction erases the whole memory (all memory bits are set to 1). The format of the instruction requires that a dummy address be provided. The Erase cycle is conducted in the same way as the Erase instruction (ERASE). The completion of the cycle can be detected by monitoring the READY/BUSY line, as described in next Section: READY/BUSY status.

Fig 6.



5. READY/BUSY status

While the Write or Erase cycle is underway, for a WRITE, ERASE, WRAL or ERAL instruction, the Busy signal (DO=0) is returned whenever Chip Select input (CS) is driven high. (Please note, though, that there is an initial delay, of t_{CS}, before this status information becomes available). In this state, the A93C46 ignores any data on the bus. When the Write cycle is completed, and Chip Select Input (CS) is driven high, the Ready signal (DO=1)

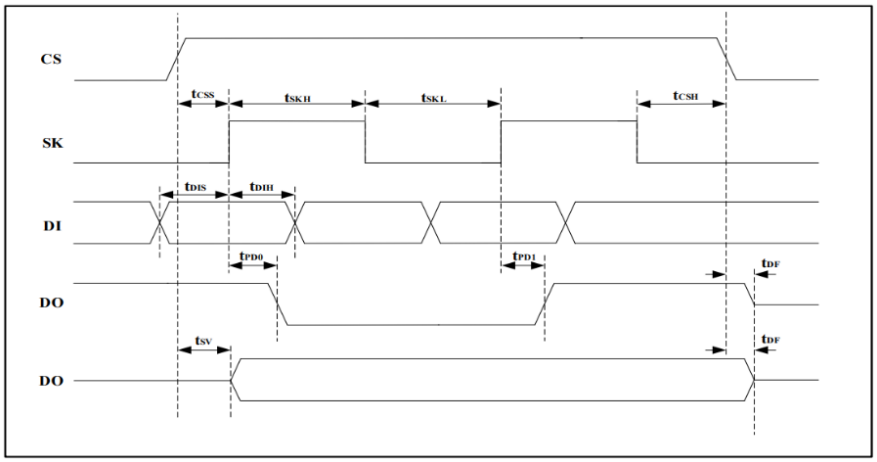
indicates that the A93C46 is ready to receive the next instruction. Serial Data Output (DO) remains set to 1 until the Chip Select Input (CS) is brought low or until a new start bit is decoded.

6. Initial Delivery State

The device is delivered with all bits in the memory array set to 1 (each byte contains FFh).

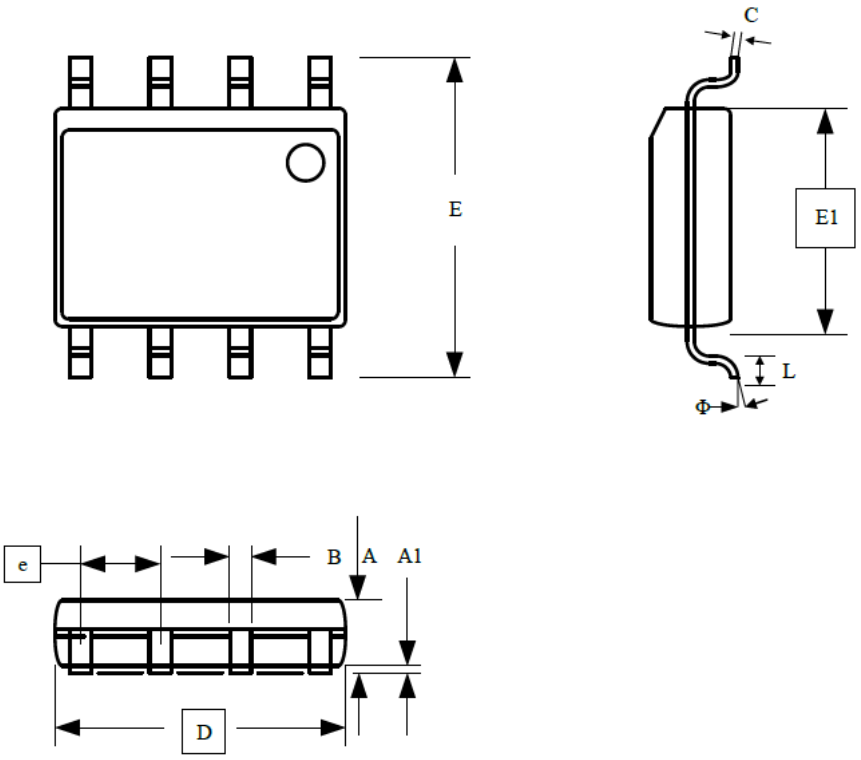
7. Synchronous Data Timing

Fig 7.



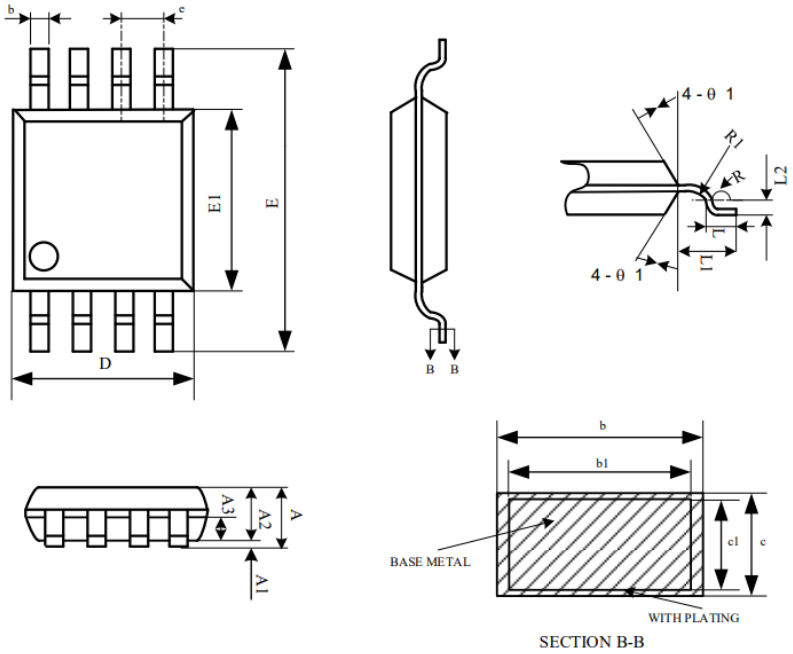
PACKAGE INFORMATION

Dimension in SOP8 (Unit: mm)



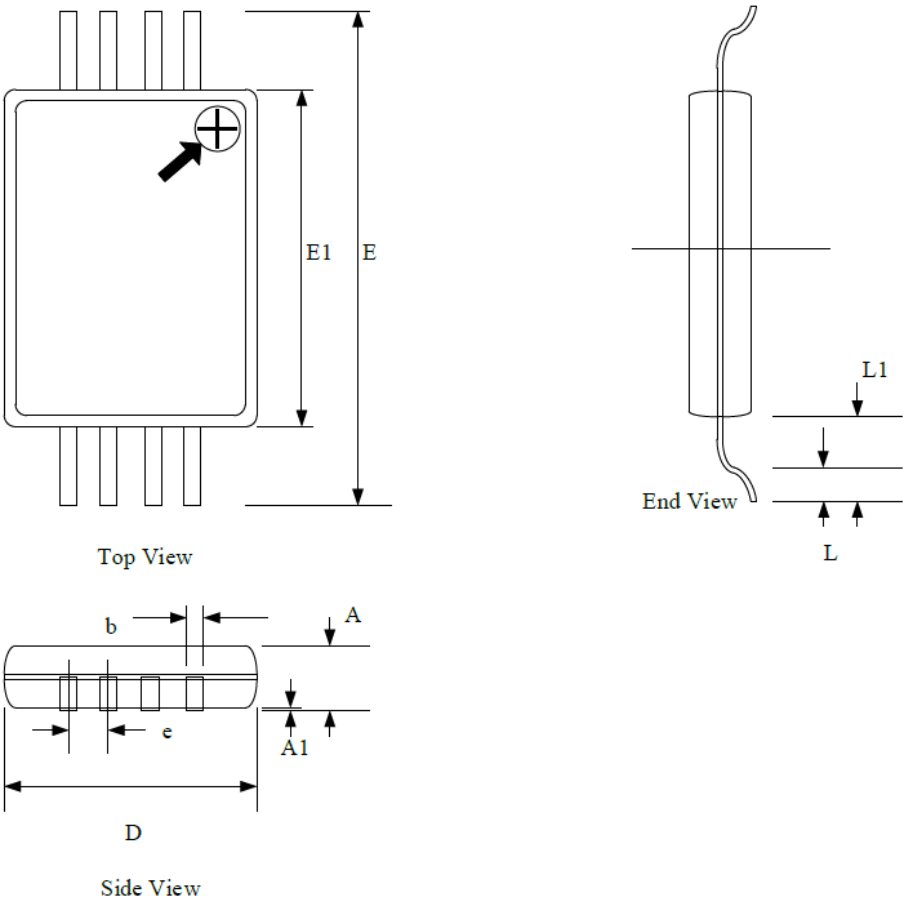
Symbol	Min	Max
A	1.350	1.750
A1	0.100	0.230
B	0.390	0.480
C	0.210	0.260
D	4.700	5.100
E1	3.700	4.100
E	5.800	6.200
e	1.270 BSC	
L	0.500	0.800
θ	0°	8°

Dimension in SSOP8 (Unit: mm)



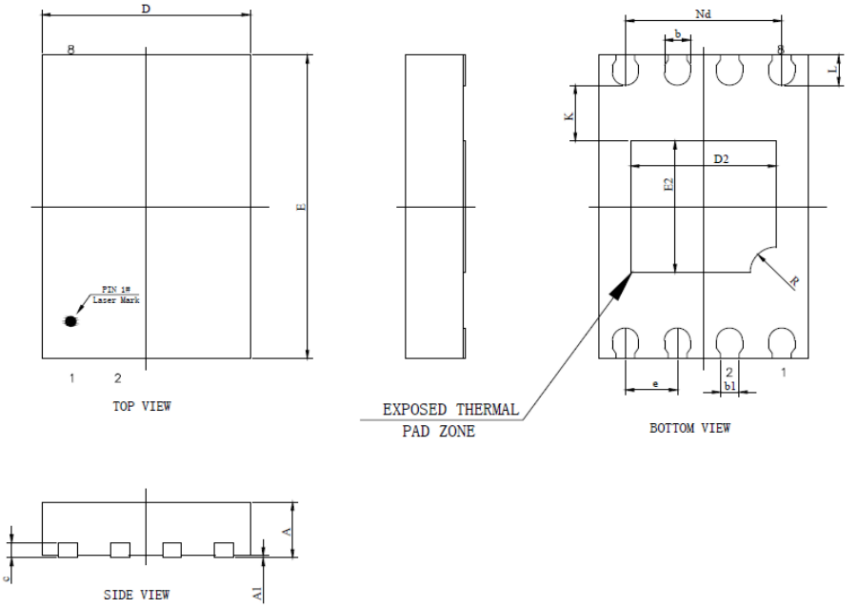
Symbol	Min	Max
A	1.000	1.300
A1	0.000	0.100
A2	1.000	1.200
A3	0.370	0.470
b	0.150	0.300
b1	0.150	0.250
c	0.110	0.200
c1	0.110	0.160
D	2.850	3.050
E	3.950	4.250
E1	2.700	2.900
e	0.550	0.750
L	0.200	0.600
L1	0.650 REF.	
L2	0.250 BSC.	
R	0.050	-
R1	0.050	-
θ	0°	8°
θ1	10°	14°

Dimension in TSSOP8 Package (Unit: mm)



Symbol	Min	Max
D	2.900	3.100
E	6.200	6.600
E1	4.300	4.500
A	-	1.200
A1	0.050	0.150
b	0.210	0.300
e	0.650 BSC	
L	0.450	0.750
L1	1.000 REF	

Dimension in DFN8 (Unit: mm)



Symbol	Min	Max
A	0.500	0.600
A1	0.000	0.050
b	0.200	0.300
b1	0.180 REF.	
c	0.152 REF	
D	1.900	2.100
D2	1.300	1.500
E	2.900	3.100
E2	1.200	1.400
e	0.500 BSC.	
Nd	1.500 BSC.	
L	0.250	0.350
R	0.200	0.300
K	0.550 REF	

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