DESCRIPTION

The AL164 is an 8-bit serial-in/parallel-out shift register. The device features two serial data inputs (A and B), eight parallel data outputs (Q0 to Q7).
Data is entered serially through A or B and either input can be used as an active High enable for data entry through the other input. Data is shifted on the Low-to-High transitions of the clock (CLK) input. A Low on the master reset input ($\overline{CLR}$) clears the register and forces all outputs Low, independently of other inputs. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of VCC.
The AL164 is available in SOP14 and TSSOP14 Packages.

FEATURES

- 8-Bit Serial Input, Parallel Output Shift
- Power-Supply Range: 1.65V to 5.5V
- Low Power Consumption: 8μA(Max)
- Low Input Current: 1μA(Max)
- Gated Serial Data Input
- Asynchronous Master Reset
- Extended Temperature: -40°C to +125°C
- Available in SOP14 and TSSOP14 Packages

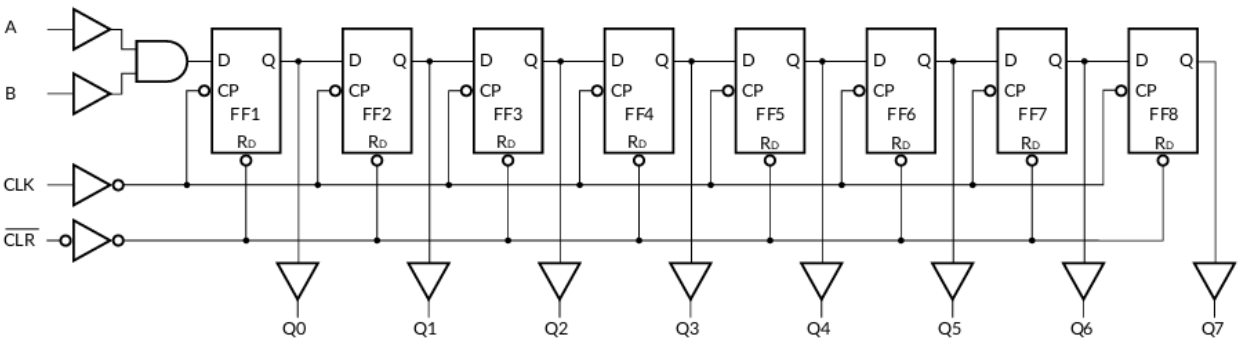
APPLICATION

- IP Routers
- Programable Logic Controllers
- Enterprise and Communications
- Industrial
- Appliances
- LED Displays
- Output Expander

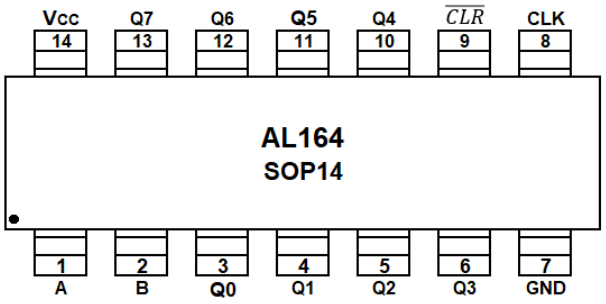
ORDERING INFORMATION

Package Type	Part Number	
SOP14 SPQ: 4,000pcs/Reel	M14	AL164M14R
		AL164M14VR
TSSOP14 SPQ:4,000pcs/Reel	TMX14	AL164TMX14R
		AL164TMX14VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

SIMPLIFIELD SCHEMATIC

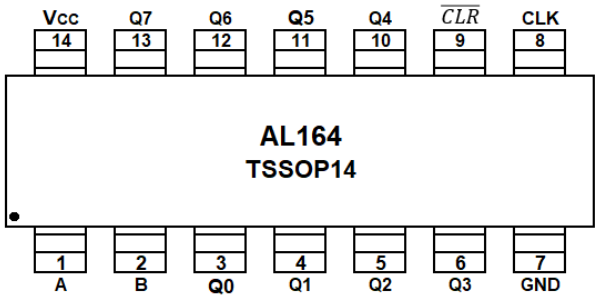


PIN DESCRIPTION



SOP14, M14

Top View



TSSOP14, TMX14

Top View

PIN#		Symbol	I/O	Function
SOP14	TSSOP14			
1	1	A	I	Data input
2	2	B	I	Data input
3	3	Q0	O	Parallel data output
4	4	Q1	O	Parallel data output
5	5	Q2	O	Parallel data output
6	6	Q3	O	Parallel data output
7	7	GND	GND	Ground
8	8	CLK	I	Clock input (Low-to-High, edge-triggered)
9	9	$\overline{CLR}$	I	Master reset (active Low)
10	10	Q4	O	Parallel data output
11	11	Q5	O	Parallel data output
12	12	Q6	O	Parallel data output
13	13	Q7	O	Parallel data output
14	14	V_{CC}	PWR	Supply voltage

FUNCTIONAL TABLE

Operating Modes	Inputs				Output	
	$\overline{CLR}$	CLK	A	B	Q0	Q1 ~ Q7
Reset (Clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

H = High voltage level

h = High voltage level one set-up time prior to the Low-to-High clock transition

L = Low voltage level

l = Low voltage level one set-up time prior to the Low-to-High clock transition

q = Lower case letters indicate the state of the referenced input one set-up time prior to the Low-to-High clock transition

↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

V_{CC}, Supply Voltage Range		-0.5V ~ + 6.5V
I_{IK}, Input Clamp Current (Max)	V_I< -0.5V or V_I > V_{CC} +0.5V	±20mA
I_{OK}, Output Clamp Current(Max)	V_I< -0.5V or V_O > V_{CC} +0.5V	±20mA
I_O, Output Current(Max)	-0.5V < V_O < V_{CC} +0.5V	±25mA
I_{CC}, Supply Current(Max)		50mA
I_{GND}, Ground Current(Min)		-50mA
θ_{JA}, Package Thermal Impedance(Max) (2)	SOP14	90°C/W
	TSSOP14	105°C/W
T_J, Junction Temperature (4)		-40℃ ~ +150℃
T_{STG}, Storage Temperature		-65℃ ~ +150℃

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) The package thermal impedance is calculated in accordance with JESD-51.

(2) The maximum power dissipation is a function of TJ(MAX), $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

ESD RATINGS

Parameter	Symbol	Min	Unit
Human-body model (HBM), MIL-STD-883K METHOD 3015.9	$V_{(ESD)}$ Electrostatic Discharge	±2000	V
Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018		±1000	
Machine Model (MM), JESD22-A115C (2010)		±200	

RECOMMENDED OPERATING CONFITIONS

TA = +25°C, Full=-40°C ~ 125°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	-	1.65	-	5.50	V
Input Voltage	V_I	-	0	-	V_{CC}	V
Output Voltage	V_O	-	0	-	V_{CC}	V
Input Transition Rise or Fall Rate (Δt / Δv)	Data Inputs	V_{CC} = 1.6V~1.95V	-	-	20	ns/V
		V_{CC} = 2.3V ~ 2.7V	-	-	20	
		V_{CC} = 3V ~ 3.6V	-	-	10	
		V_{CC} = 4.5V ~5.5V	-	-	5	
Operating Temperature	T_A	-	-40	-	+125	°C

* All unused inputs of the device must be held at VCC or GND to ensure proper device operation.

ELECTRICAL CHARACTERISTICS

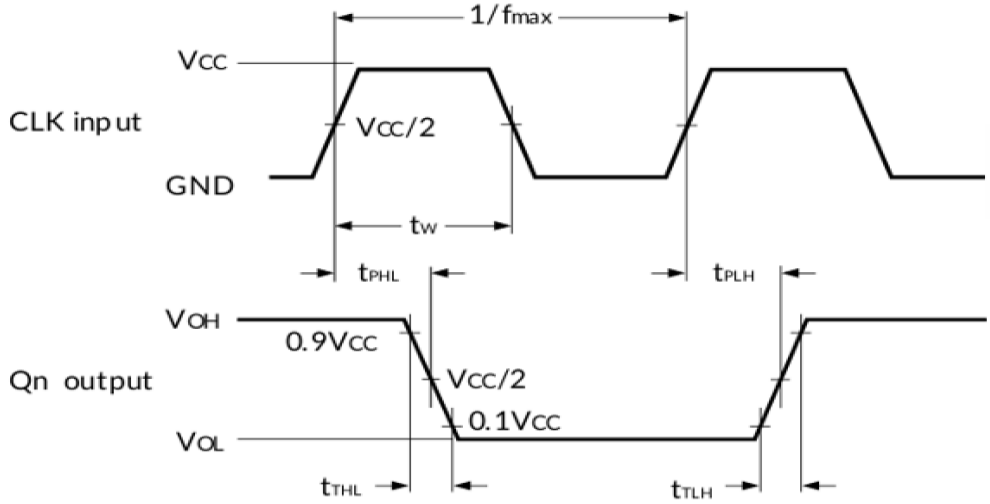
Parameter		Conditions		Min	Typ.	Max	Unit
High-Level Input Voltage	V_{IH}	V_{CC}=1.65V~1.95V	-65°C ~ +150°C	0.7xV_{CCI}	-	-	V
		V_{CC}=2.3V~2.7V		1.70	-	-	
		V_{CC}=3V~3.6V		2	-	-	
		V_{CC}=4.5V~5.5V		0.7xV_{CCI}	-	-	
Low-Level Input Voltage	V_{IL}	V_{CC}=1.65V~1.95V	-65°C ~ +150°C	-	-	0.3xV_{CCI}	V
		V_{CC}=2.3V~2.7V		-	-	0.70	
		V_{CC}=3V~3.6V		-	-	0.80	
		V_{CC}=4.5V~5.5V		-	-	0.3xV_{CCI}	
High-Level Output Voltage V_I = V_{IH} or V_{IL}	V_{OH}	I_O = -100μA, V_{CC}=1.65V~5.5V	-65°C ~ +150°C	V_{CC}-0.1	-	-	V
		I_O = -4mA, V_{CC}=3V		1.20	-	-	
		I_O = -8mA, V_{CC}=3.3V		1.90	-	-	
		I_O = -10mA, V_{CC}=5.5V		3.80	-	-	
Low-Level Output Voltage V_I = V_{IH} or V_{IL}	V_{OL}	I_O = 100μA, V_{CC}=1.65V~5.5V	-65°C ~ +150°C	-	-	0.10	V
		I_O = 4mA, V_{CC}=3V		-	-	0.45	
		I_O = 8mA, V_{CC}=3.3V		-	-	0.40	
		I_O = 10mA, V_{CC}=5.5V		-	-	0.55	
Input Leakage Current	I_I	V_I = 5.5V or GND, V_{CC}=0V~5.5V	-65°C ~ +150°C	-	-	±1	μA
Supply Current	I_{CC}	V_I = 5.5V or GND, I_O=0, V_{CC}=0V~5.5V	-65°C ~ +150°C	-	-	8	
Input Capacitance	C_I	-	+25°C	-	6	-	pF

SWITCHING CHARACTERISTICS

Symbol	Parameter	Test Conditions	25°C (1)			-40°C To +125°C (1)			Unit
			Min	Typ	Max	Min	Typ	Max	
t_{pd} (2)	Propagation delay CLK to Qn	V_{CC}=1.8V±0.15V	-	34	-	-	-	68	ns
		V_{CC}=2.5V±0.2V	-	24	-	-	-	58	
		V_{CC}=3.3V±0.3V	-	18	-	-	-	36	
		V_{CC}=5V±0.5V	-	14	-	-	-	28	
t_{PHL}	High to Low propagation delay	$\overline{CLR}$ to Qn							
		V_{CC}=1.8V±0.15V	-	24	-	-	-	48	ns
		V_{CC}=2.5V±0.2V	-	14	-	-	-	28	
		V_{CC}=3.3V±0.3V	-	10	-	-	-	20	
		V_{CC}=5V±0.5V	-	8	-	-	-	16	
t_t (3)	transition time	V_{CC}=1.65V	-	19	-	-	-	60	ns
		V_{CC}=4.5V	-	7	-	-	-	22	
		V_{CC}=5.5V	-	6	-	-	-	20	
t_w	Pulse width	CLK High or Low							
		V_{CC}=1.65V	110	-	-	110	-	-	ns
		V_{CC}=4.5V	22	-	-	22	-	-	
		V_{CC}=5.5V	19	-	-	19	-	-	
		CLR LOW							
		V_{CC}=1.65V	110	-	-	110	-	-	ns
		V_{CC}=4.5V	22	-	-	22	-	-	
		V_{CC}=5.5V	19	-	-	19	-	-	
t_{rec}	Recovery time	$\overline{CLR}$ to CLK							
		V_{CC}=1.65V	50	-	-	50	-	-	ns
		V_{CC}=4.5V	10	-	-	10	-	-	
		V_{CC}=5.5V	9	-	-	9	-	-	
t_{su}	Set-up time	A, and B to CLK							
		V_{CC}=1.65V	55	-	-	55	-	-	ns
		V_{CC}=4.5V	11	-	-	11	-	-	
		V_{CC}=5.5V	10	-	-	10	-	-	
t_h	Hold width	A, and B to CLK							
		V_{CC}=1.65V	3	-	-	3			ns
		V_{CC}=4.5V	3	-	-	3			
		V_{CC}=5.5V	3	-	-	3			
f_{max}	Maximum frequency	For CLK							
		V_{CC}=1.65V	4	-	-	4	-	-	MHz
		V_{CC}=4.5V	20	-	-	20	-	-	
		V_{CC}=5.5V	24	-	-	24	-	-	
C_{PD} (4)	Power dissipation capacitance	per package; V_I = GND to V_{CC}	-	115	-	-	-	-	pF

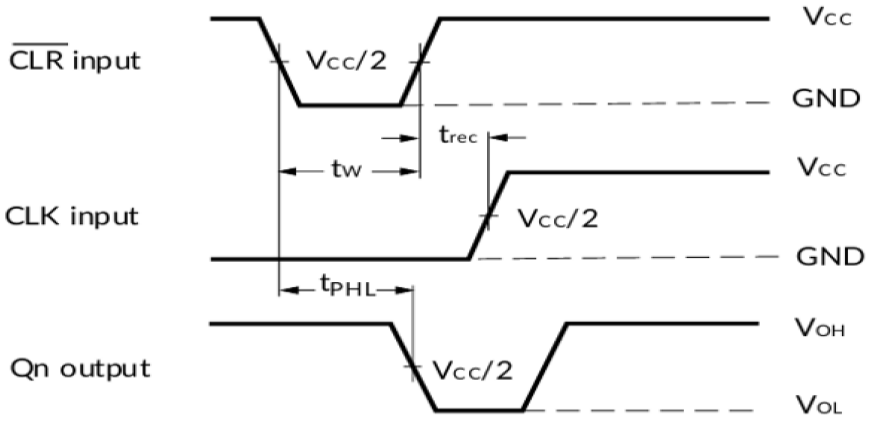
(1) This parameter is ensured by design and/or characterization and is not tested in production.
(2) t_{pd} is the same as t_{PHL} and t_{PLH}.
(3) t_t is the same as t_{THL} and t_{TLH}.
(4) C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_O)$ where:
f_i = input frequency in MHz;
f_O = output frequency in MHz.
$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs.
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching.

PARAMETER MEASUREMENT INFORMATION



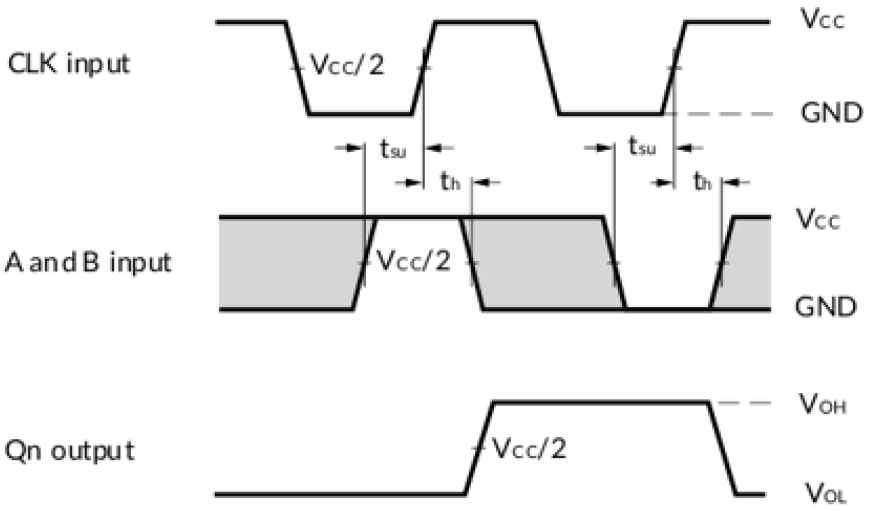
OL and VOH are typical voltage output levels that occur with the output load.

Fig1. Waveforms showing the clock (CLK) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency



VOL and VOH are typical voltage output levels that occur with the output load.

Fig2. Waveforms showing the master reset ($\overline{CLR}$) pulse width
the master reset to output (Qn) propagation delays and the master reset to clock (CLK) removal time



VOL and VOH are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance

Fig3. Waveforms showing the data set-up and hold times for A and B inputs

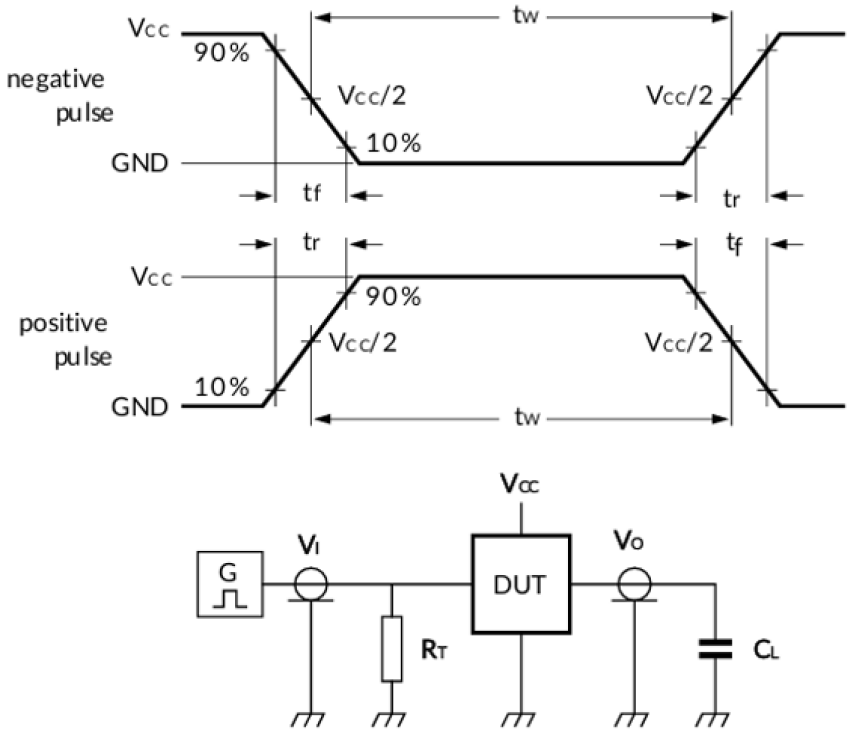


Fig4. Test circuit for measuring switching times

Test data is given in Table 1.

Definitions test circuit:

R_T = termination resistance should be equal to output impedance Zo of the pulse generator.

C_L = load capacitance including jig and probe capacitance

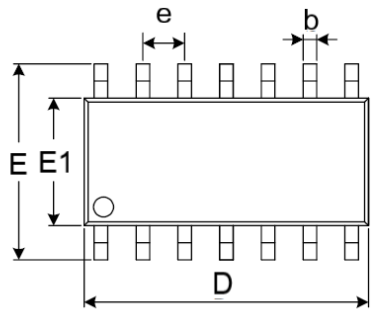
TEST DATA

Test	Input		Load
	V_I	t_r, t_f	C_L
t_{PHL}/t_{PLH}	V_{CC}	6ns	15pF, 50pF

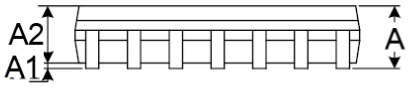
Table 1. Test data

PACKAGE INFORMATION

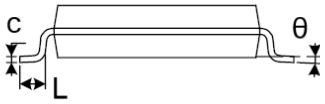
Dimension in SOP14 (Unit: mm)



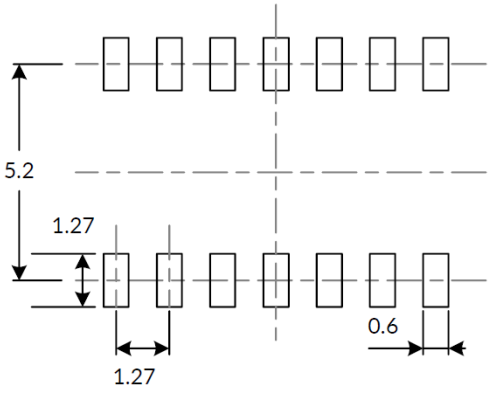
TOP VIEW



BOTTOM VIEW



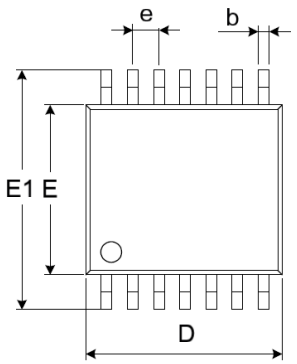
SIDE VIEW



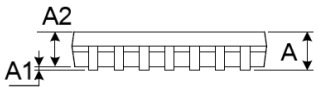
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Millimeters	
	Min	Max
A	-	1.750
A1	0.100	0.250
A2	1.350	1.500
b	0.390	0.470
c	0.200	0.240
D	8.550	8.750
e	1.270 BSC	
E	5.800	6.200
E1	3.800	4.000
L	0.500	0.800
θ	0°	8°

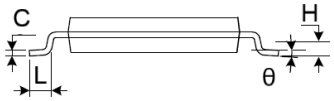
Dimension in TSSOP14 (Unit: mm)



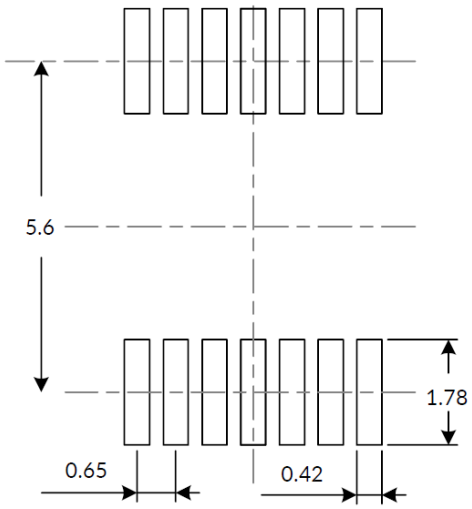
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Millimeters	
	Min	Max
A	-	1.200
A1	0.500	0.150
A2	0.900	1.050
b	0.200	0.300
c	0.130	0.170
D	4.860	5.100
E	4.300	4.500
E1	6.200	6.600
e	0.650 BSC	
L	0.500	0.700
H	0.25 TYP	
θ	0°	8°

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