DESCRIPTION

The AL175 is a quad positive-edge-triggered D-type flip-flop with individual data inputs (nD) and complementary outputs (nQ and nQ). The common clock (CLK) and master reset (CLR) inputs control all flip-flops simultaneously. Data that meet the setup and hold time requirements on the LOW-to-HIGH transition of the clock input will be stored in the flip-flop and appear at the Q output.

A LOW level on CLR resets all flip-flops and forces the outputs LOW. The inputs include clamp diodes, allowing the use of current-limiting resistors to interface inputs to voltages higher than V_{CC}.

This device operates over an ambient temperature range of −40 °C to +125 °C.

AL175 is available in SOP16 and TSSOP16 packages.

FEATURES

- Operating Voltage Range: 1.65V to 5.5V
- Low Power Consumption: 8μA (Max)
- Four edge-triggered D-type flip-flops
- Asynchronous master reset
- Operating Temperature Range: -40°C ~ +125°C
- Available in SOP16 and TSSOP16 packages

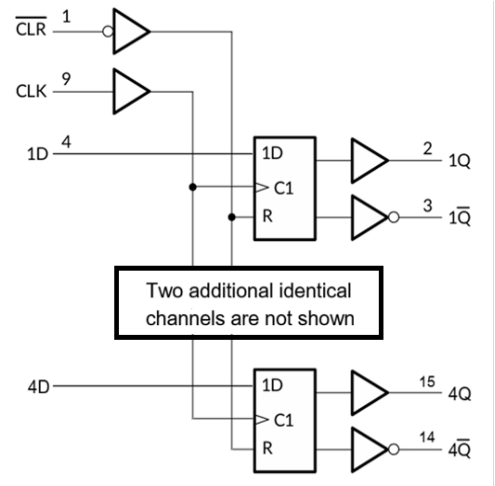
APPLICATION

- Buffer/Storage Registers
- Shift Registers
- Pattern Generators

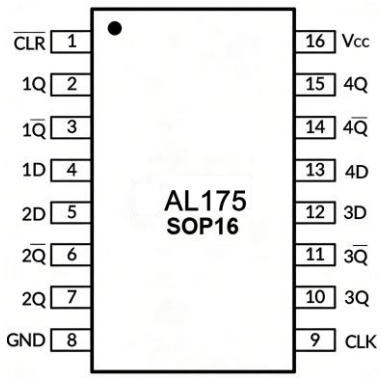
ORDERING INFORMATION

Package Type	Part Number	
SOP16 SPQ: 4,000pcs/Reel	M16	AL175M16R
		AL175M16VR
TSSOP16 SPQ: 4,000pcs/Reel	TMX16	AL175TMX16R
		AL175TMX16VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

LOGIC SYMBOL

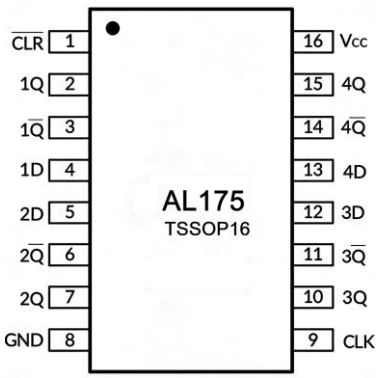


PIN DESCRIPTION



SOP16, M16

Top View



TSSOP16, TMX16

Top View

PIN#		Symbol	I/O Type	Function
SOP16	TSSOP16			
1	1	$\overline{CLR}$	I	Clear Data Input
2	2	1Q	O	Output
3	3	$1\overline{Q}$	O	Output
4	4	1D	I	Input
5	5	2D	I	Input
6	6	$2\overline{Q}$	O	Output
7	7	2Q	O	Output
8	8	GND	P	Ground
9	9	CLK	I	Clock Input
10	10	3Q	O	Output
11	11	$3\overline{Q}$	O	Output
12	12	3D	I	Input
13	13	4D	I	Input
14	14	$4\overline{Q}$	O	Output
15	15	4Q	O	Output
16	16	V_{CC}	P	Power Pin

FUNCTION TABLE

INPUT			OUTPUT	
$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q0	$\overline{Q}0$

H: High Voltage Level

L: Low Voltage Level

X: Don't care

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

V_{CC}, Supply Voltage Range		-0.5V ~ + 6.5V
I_{IK}, Input Clamp Current	V_I < 0V or V_I > V_{CC}	±20mA
I_{OK}, Output Clamp Current	V_O < 0V or V_O > V_{CC}	±20mA
I_O, Continuous Output Current	V_O = 0V ~ V_{CC}	±25mA
I_O, Continuous Current through V_{CC} or GND		±50mA
θ_{JA}, Package Thermal Impedance (2)	SOP16	150°C/W
	TSSOP16	45°C/W
T_J, Junction Temperature (3)		-65℃ ~ +150℃
T_{STG}, Storage Temperature		-65℃ ~ +150℃
$V_{(ESD)}$, Electrostatic Discharge	Human-body model (HBM), MIL-STD-883K METHOD 3015.9	±2000V
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±1000V
	Machine Model (MM), JESD22-A115	±200V

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(2) The package thermal impedance is calculated in accordance with JESD-51.

(3) The maximum power dissipation is a function of TJ(MAX), $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

RECOMMENDED OPERATING CONFITIONS

T_A=25°C, Full=-40°C to 125°C,unless otherwise noted.*

Parameter	Symbol	Conditions	Min	Typ.	Max	Unit
Supply Voltage	V_{CC}	Operating	1.65	-	5.50	V
High-Level Input Voltage	V_{IH}	V_{CC} = 2.0V	1.50	-		
		V_{CC} = 3.3V	2.40	-		
		V_{CC} = 4.5V	3.15	-		
		V_{CC} = 5.5V	3.85	-		
Low-Level Input Voltage	V_{IL}	V_{CC} = 2.0V	-	-	0.50	V
		V_{CC} = 3.3V	-		1.00	
		V_{CC} = 4.5V	-		1.35	
		V_{CC} = 5.5V	-		1.65	
Input Voltage	V_I	-	0	-	V_{CC}	V
Output Voltage	V_O	-	0	-	V_{CC}	V
Input Transition Rise or Fall	Δt/Δv	V_{CC} = 2.0V	-	-	1000	ns
		V_{CC} = 3.3V	-	-	600	
		V_{CC} = 4.5V	-	-	500	
		V_{CC} = 5.5V	-	-	400	
Operating Temperature	T_A	-	-40	-	+125	°C

*All unused inputs of the device must be held at VCC or GND to ensure proper device operation.

DC CHARACTERISTICS

Parameter		Conditions		Min	Typ.	Max	Unit
V_{OH}		I_{OH} = -20μA, V_{CC}=2.0V	-40℃ ~ +125℃	1.90	-	-	V
		I_{OH} = -20μA, V_{CC}=3.3V		3.20	-	-	
		I_{OH} = -20μA, V_{CC}=4.5V		4.40	-	-	
		I_{OH} = -20μA, V_{CC}=5.5V		5.40	-	-	
		I_{OH} = -4mA, V_{CC}=4.5V		3.84	-	-	
		I_{OH}= -5.2mA, V_{CC}=5.5V		4.69	-	-	
V_{OL}		I_{OL} = 20μA, V_{CC}=2.0V	-40℃ ~ +125℃	-	-	0.10	V
		I_{OL} = 20μA, V_{CC}=3.3V		-	-	0.10	
		I_{OL} = 20μA, V_{CC}=4.5V		-	-	0.10	
		I_{OL} = 20μA, V_{CC}=5.5V		-	-	0.10	
		I_{OL} = 4.0mA, V_{CC}=4.5V		-	-	0.50	
		I_{OL}= 5.2mA, V_{CC}=5.5V		-	-	0.55	
I_I		V_I = 5.5V or GND, V_{CC}=5.5V	+25℃	-	±0.1	±1	μA
			-40℃ ~ +125℃	-	-	±2	
I_{CC}		V_I = 5.5V or GND, I_O=0, V_{CC}=5.5V	+25℃	-	-	8	μA
			-40℃ ~ +125℃	-	-	80	
Ci	Input Capacitance	V_{CC}=1.65V ~ 5.5V	+25℃	-	4	10	pF
			-40℃ ~ +125℃	-	-	10	

(1) All unused inputs of the device must be held at VCC or GND to ensure proper device operation

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, CL = 50 pF (unless otherwise noted) (1)

Parameter		Conditions	T_A = 25°C			T_A=-40°C~ 125°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{max}		V_{CC} = 2.0V	6	12	-	5	-	-	MHz
		V_{CC} = 3.3V	18	30	-	15	-	-	
		V_{CC} = 4.5V	31	50	-	25	-	-	
		V_{CC} = 5.5V	33	55	-	27	-	-	
t_{pd}, $\overline{CLR}$	Any	V_{CC} = 2.0V	-	17	25.5	-	-	28.8	ns
		V_{CC} = 3.3V	-	8	12	-	-	13.5	
		V_{CC} = 4.5V	-	6	9	-	-	10	
		V_{CC} = 5.5V	-	5.5	8.5	-	-	9.5	
t_{pd}, CLK	Any	V_{CC} = 2.0V	-	23.5	35	-	-	39	
		V_{CC} = 3.3V	-	10.5	16	-	-	18	
		V_{CC} = 4.5V	-	8.5	13	-	-	13.5	
		V_{CC} = 5.5V	-	7.5	11.5	-	-	12	
t_r	Any	V_{CC} = 2.0V	-	10.5	15.5	-	-	18	ns
		V_{CC} = 3.3V	-	5.5	8.5	-	-	10	
		V_{CC} = 4.5V	-	4.5	7	-	-	8.5	
		V_{CC} = 5.5V	-	4	6	-	-	7.5	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

OPERATING CHARACTERISTICS

T_A=25°C

Parameter		Conditions	Min	Typ.	Max	Unit
C_{pd}	Power dissipation capacitance per flip-flop	No load	-	35	-	pF

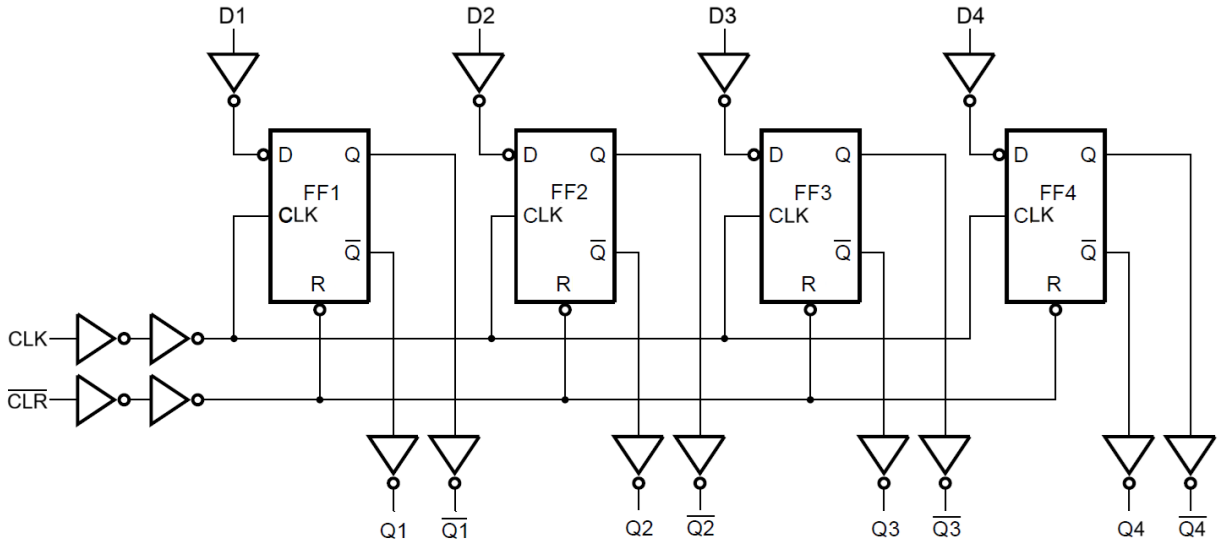
TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (1)

Parameter		Conditions	T_A = 25°C			T_A=-40°C~ 125°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{clock}	Clock frequency	V_{CC} = 2.0V	-	-	6	-	-	5	MHz
		V_{CC} = 3.3V	-	-	18	-	-	15	
		V_{CC} = 4.5V	-	-	31	-	-	25	
		V_{CC} = 5.5V	-	-	33	-	-	27	
t_w, Pulse duration	$\overline{CLR}$ low	V_{CC} = 2.0V	40	-	-	52	-	-	ns
		V_{CC} = 3.3V	20	-	-	30	-	-	
		V_{CC} = 4.5V	8	-	-	10	-	-	
		V_{CC} = 5.5V	6	-	-	8	-	-	
t_w, Pulse duration	CLK High or low	V_{CC} = 2.0V	40	-	-	52	-	-	
		V_{CC} = 3.3V	20	-	-	30	-	-	
		V_{CC} = 4.5V	8	-	-	10	-	-	
		V_{CC} = 5.5V	6	-	-	8	-	-	
t_{su}, Setup time before CLK ↑	Data	V_{CC} = 2.0V	50	-	-	65	-	-	ns
		V_{CC} = 3.3V	30	-	-	38	-	-	
		V_{CC} = 4.5V	10	-	-	12	-	-	
		V_{CC} = 5.5V	8	-	-	10	-	-	
	$\overline{CLR}$ inactive	V_{CC} = 2.0V	50	-	-	65	-	-	
		V_{CC} = 3.3V	30	-	-	38	-	-	
		V_{CC} = 4.5V	10	-	-	12	-	-	
		V_{CC} = 5.5V	8	-	-	10	-	-	
t_h Hold time, data after CLK ↑		V_{CC} = 2.0V	-	6.1	-	-	-	-	ns
		V_{CC} = 3.3V	-	2.6	-	-	-	-	
		V_{CC} = 4.5V	-	2	-	-	-	-	
		V_{CC} = 5.5V	-	1.8	-	-	-	-	

(1) This parameter is ensured by design and/or characterization and is not tested in production.

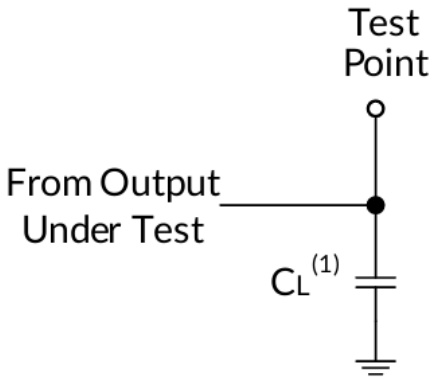
BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION

The phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators with the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, and t_t < 6 ns. For clock inputs, f_{max} is measured with an input duty cycle of 50%. The outputs are measured one at a time, with one input transition per measurement.

Fig 1. Load Circuit for Push-Pull Outputs



(1) C_L includes probe and test-fixture capacitance.

Fig 2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

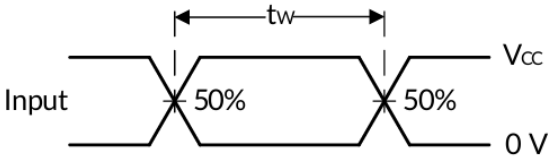


Fig 3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times

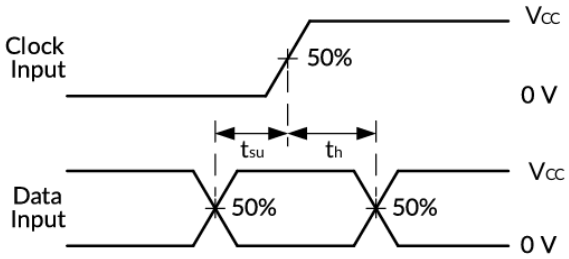
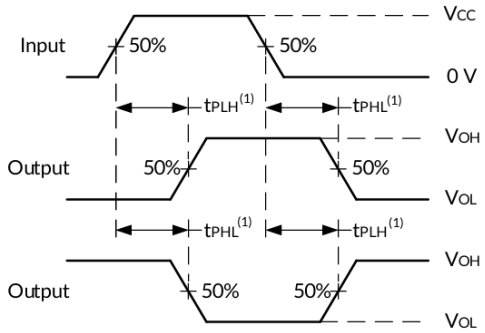
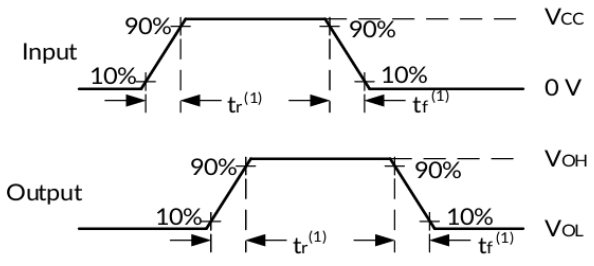


Fig 4. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

Fig 5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t.

DETAILED DESCRIPTION

Overview

These positive-edge-triggered D-type flip-flops feature a direct clear ($\overline{CLR}$) input. The AL175 devices provide complementary outputs from each flip-flop.

Data present at the data (D) inputs that meet the setup time requirements are transferred to the outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a specified voltage level and is not directly related to the transition time of the positive-going edge of CLK.

Power Supply Recommendations

The power supply voltage can be of any value within the minimum and maximum limits specified in the Recommended Operating Conditions. Each V_{CC} terminal should be properly bypassed with a capacitor to prevent power supply disturbances. A 0.1 μF bypass capacitor is recommended for this device.

Multiple bypass capacitors may be connected in parallel to suppress noise over a wide frequency range. A combination of 0.1 μF and 1 μF capacitors is commonly used. For best performance, the bypass capacitors should be placed as close as possible to the V_{CC} terminal.

Layout Guidelines

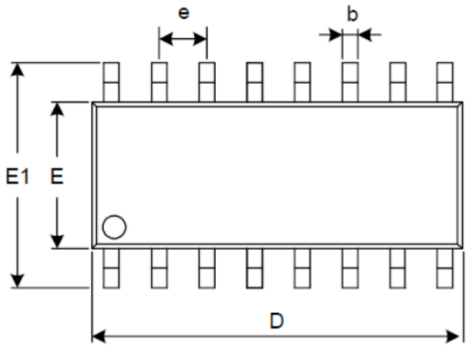
When using multi-input or multi-channel logic devices, inputs must never be left floating. In many applications, some functions or portions of a digital logic device may remain unused. For example, only two inputs of a triple-input AND gate may be used, or only three of the four buffer gates may be utilized.

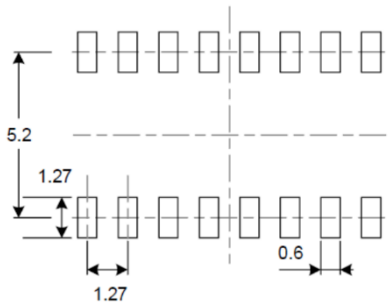
Unused input pins must not be left unconnected because undefined voltages at these inputs can lead to unpredictable or undefined operating states. All unused inputs of digital logic devices should be connected to a valid logic HIGH or logic LOW level, as defined by the input voltage specifications, to prevent them from floating.

The logic level applied to an unused input depends on the function of the device. In general, unused inputs are tied to either GND or V_{CC}, whichever is more appropriate for the logic function or more convenient in the circuit design.

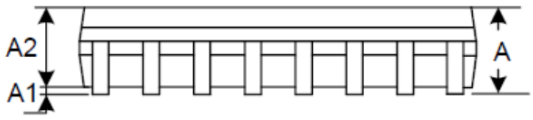
PACKAGE INFORMATION

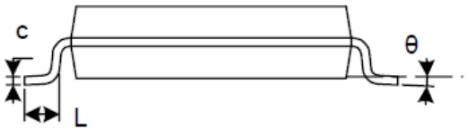
Dimension in SOP16 (Unit: mm)





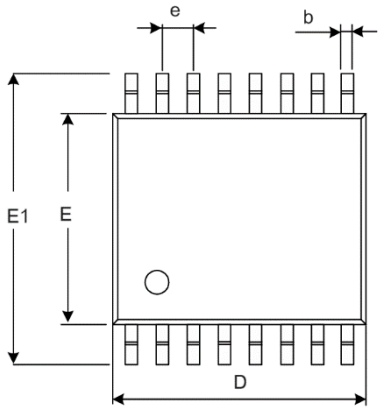
RECOMMENDED LAND PATTERN

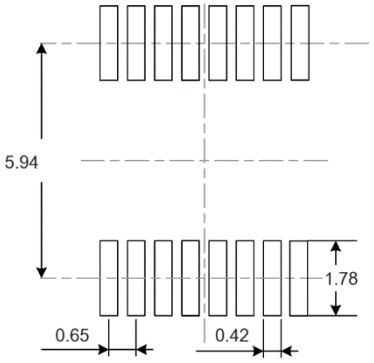




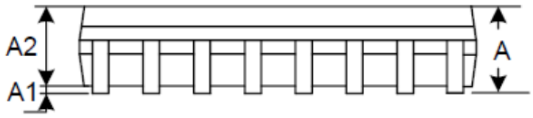
Symbol	Millimeters	
	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	9.800	10.200
E	3.800	4.000
E1	5.800	6.200
e	1.270 BSC.	
L	0.400	1.270
θ	0°	8°

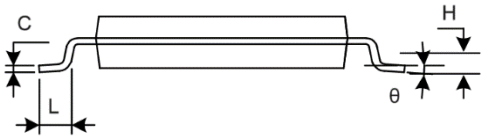
Dimension in TSSOP16 (Unit: mm)





RECOMMENDED LAND PATTERN





Symbol	Millimeters	
	Min	Max
A	-	1.200
A1	0.050	0.150
A2	0.800	1.050
b	0.190	0.300
c	0.090	0.200
D	4.860	5.100
E	4.300	4.500
E1	6.200	6.600
e	0.650 BSC.	
L	0.500	0.700
H	0.250 TYP.	
θ	1°	7°

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