DESCRIPTION

The AP8275 is a highly integrated flyback PWM controller with a maximum switching frequency of 85 kHz.

It incorporates multiple advanced features to enhance overall power supply performance. The controller operates in continuous conduction mode (CCM) under heavy load conditions and transitions to valley switching mode at light load. At extremely light load, it further enters burst mode to improve efficiency.

With an integrated high-voltage startup circuit and built-in X-capacitor discharge function, no external startup resistor or X-cap discharge resistor is required. This significantly reduces component count and enables ultra-low input standby power consumption.

The AP8275 is available in SOP8 package

APPLICATION

- USB Power Delivery (PD) and Programmable Power Supplies (PPS)
- Switching AC/DC Adapters and Battery Chargers
- Open-frame Switching Power Supplies

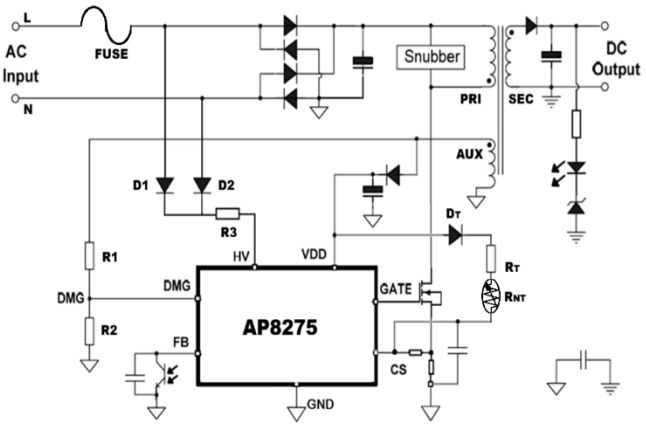
ORDERING INFORMATION

Package Type	Part Number	
SOP8 SPQ: 4,000pcs/Reel	M8	AP8275M8VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products		

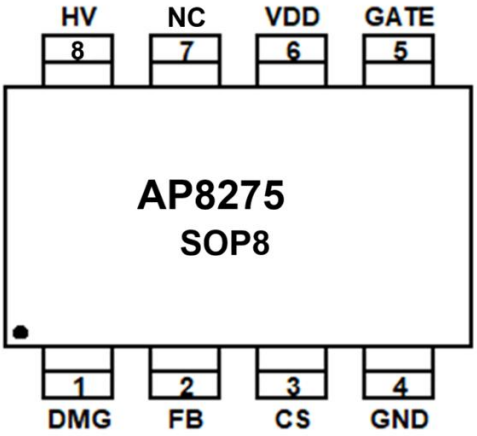
FEATURES

- Integrated 700 V high-voltage startup circuit
- Wide V_{CC} operating range: 10 V to 80 V
- Low standby power consumption (<30 mW)
- Brown-in / Brown-out and X-capacitor discharge via HV pin
- Multi-mode operation: current-mode control, CCM, and valley switching
- Auto-tuned current sense (CS) limit for wide output range applications
- Two-step CS limit for peak load capability
- Line voltage compensation for constant over-power protection (OPP)
- Frequency jittering for reduced EMI
- Built-in slope compensation
- 6 ms soft-start time
- Programmable external OTP
- Programmable DEM OVP / UVP
- Short-circuit protection (SCP)
- Secondary synchronous rectifier SCP (SRSP)
- Feedback open-loop protection (FB OLP)
- V_{CC} over-voltage protection (OVP)
- Internal OTP
- Meets LPS requirements
- Adaptive V_{CC} self-recovery protection to reduce input power consumption

TYPICAL APPLICATION



PIN DESCRIPTION



SOP8, M8

Top View

Pin #	Symbol	Function
1	DMG	Valley detection pin, adjusts output OVP.
2	FB	Voltage feedback. By connecting a photo-coupler to close the control loop and achieve the regulation.
3	CS	Current Sense Input
4	GND	Ground
5	GATE	Totem-pole gate drive output for the power MOSFET.
6	V_{DD}	Positive Supply voltage Input
7	NC	No Connection
8	HV	High voltage start pin. High voltage startup, X-cap discharge and AC Brown-in/out protection is realized by connecting diodes to AC input.

ABSOLUTE MAXIMUM RATINGS

Supply voltage Pin V_{DD}		-0.3V ~ 91V
FB, CS, DMG Pin		-0.3V ~ 7V
GATE Pin		-0.3V ~ 16V
HV Pin		-0.3V ~ 700V
Operating Junction Temperature℃		-40℃~ 150℃
Storage Temperature Range		-65℃~ 150℃
Lead Temperature (Soldering, 10Secs)		260℃
Package Thermal Resistance	SOP8	80℃/W
Maximum power Dissipation		1W
Junction to Ambient ($R_{\theta JA}$)		128°C/W
Junction to Case ($R_{\theta JC}$)		90°C/W

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING

Operating Temperature (Environment)	-40℃~ 125℃
V_{DD} Supply Voltage	8.3V~80V
Startup Resistor	10kΩ ~20kΩ
V_{DD} Capacitor	2.2μF~4.7μF
CS pin Capacitor	220pF~680pF
CS Pin Filter Resistor	100Ω ~680Ω
FB pin Capacitor	470pF~4.7nF

ELECTRICAL CHARACTERISTICS

T_A=25°C, V_{DD}=15V, unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HV Section						
Break-Down Voltage	BV_{HV}	I_{HV}=250μA	-	700	-	V
HV Start Up Charging Current	$I_{\_HV1}$	V_{DD}<V_{DD_oN}, HV=50V~400V	-	3	-	mA
HV Off-State Current	$I_{\_HV2}$	1V>V_{DD}, HV=50V~400V	-	0.5	1	mA
HV Leakage current	I_{HVLK}	V_{DD}> V_{DD_ON}, HV=400V		10	15	μA
X-Cap Discharge Current	I_{DISCX}		-	5	-	mA
X-cap discharge detection delay time	t_{D_X}			47		ms
X-cap discharge time	t_{DISCX}			47		ms
HV Section- Brown/in out						
Brown In Voltage	$V_{\_BNI}$		90	100	110	V
Brown Out Voltage	$V_{\_BNO}$		81	90	99	V
Brown Out Debounce Duration	T_{DB_BNO}	Time for V_{HV}<$V_{\_BNO}$	-	105	-	ms
V_{DD} Supply Section						
V_{DD} Start Up Threshold	V_{DD_on}		16	17	18	V
V_{DD} Under Voltage Shutdown Threshold	V_{DD_off}		9.0	9.5	10.0	V
V_{DD} OVP Voltage	V_{DD_ovp}		82	85	88	V
De-Bounce time of V_{DD} OVP Voltage	T_{DB_OVP}		-	5	-	cycles
V_{DD} Holdup level	V_{DD_HD}	V_{FB}<V_{ZD_OFF}	1.1xV_{DD_OFF}			V
Auto Recovery time	t_{REC_A}	Except BNO and V_{DD_OFF}	-	8	-	times
Operating Current	I_{OP}	V_{FB}=2V,GATE=1nF F_{SW}=85KHz		1.5		mA
		V_{FB}<V_{ZD_OFF}		400	500	μA
Protection Mode Current	I_{PRO}	V_{DD}> V_{DD_OFF}	400	550	700	μA
OSCILLATOR Section						
Switching Frequency	f_{SW}		80	85	90	kHz
Green Mode Freqency	f_{GM}		18	25	32	kHz
Frequency Spreading Range	f_{SPR}	f_{SW}@85kHz, V_{FB}>$V_{G\_IN\_H}$	-	±6.0	-	kHz
		f_{SW}@25kHz, V_{FB}>$V_{G\_IN\_L}$		±1.75		kHz
Spreading Frequency	f_{SP}		-	330	-	Hz
Maximum Duty Cycle	D_{MAX}		73	78	83-	%

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
FB Section						
Soft Start Time	t_{SS}	$V_{HV}>V_{BNI}$		6		ms
FB pin Short Current	I_{SC_FB}			145		μA
FB to CS Attenuation	A_V			1/3		V/V
Open Loop Voltage	$V_{OPEN-LOOP}$			5.1		V
Green in Level (High level)	$V_{G\_IN\_H}$			1.7		V
Green out Level (High level)	$V_{G\_OUT\_H}$			1.2		V
Green in Level (Low level)	$V_{G\_IN\_L}$			1.5		V
Green out Level (Low level)	$V_{G\_OUT\_L}$			1.02		V
Zero duty Cycle ON	V_{ZD_ON}			0.8		V
Zero duty Cycle OFF	V_{ZD_OFF}			0.6		V
FB Startup Level	V_{FB_ST}			1.3		V
OLP Trigger threshold	V_{OLP}		3.8	4.0	4.2	V
OLP Debounce time	t_{DB_OLP}			105		ms
Current Sense Section						
OPP(Hard limit for Peak Load)	V_{OPP}	I_{DMG}<340μA, CS limit =0.8V		0.80		V
		I_{DMG}>350μA, CS limit =0.8V		0.6		V
OCP Threshold	V_{OCP}	$V_{DMG}\geqslant$3.1V		0.58		V
		$V_{DMG}\leqslant$0.8V		0.45		V
OCP Delay Time	t_{D_OCP}	f_{SW}@85kHz, $V_{CS}>V_{OCP}$		105		ms
OCP Reset Counter	C_{R_OCP}	$V_{CS}<V_{OCP}$	16			cycle
Output SCP Debounce Time	t_{DB_SCP}	$V_{DD}=V_{DD\_HD}$, $V_{CS}>V_{OCP}$, over 7 cycles		7		cycle
OCP Compensation Current for AC Input Voltage	I_{COMP_OCP}	DMG source Current = 100μA		66.7		μA
Leading Edge Blanking (LEB) Time	t_{LEB}			250		ns
Propagation Delay Time	t_{D_PPG}			100		ns
CS OTP Threshold	V_{CS_OTP}			0.55		V
CS OTP Debounce Time	$t_{DB\_CS\_OTP}$			5		cycle
CS OTP Blanking Time	$t_{LEB\_CS\_OTP}$			1.2		μs
CS SRSP Threshold	V_{SRSP}			1		V
CS SRSP Debounce Time	t_{DB_SRSP}			7		times
Slope Compensation	V_{SLOPE}	Duty cycle = Maximum ON time		300		mV

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DMG Section						
Detection Level	V_{DMG}			150		mV
Timeout for Last Detection Signal	t_{TO_DMG}			2.5		μs
DMG OVP Voltage	V_{DMG_OVP}		3.8	4.0	4.2	V
DMG OVP blanking time	$t_{LEB\_DEM\_OVP}$		1.0	1.2	1.4	μs
De-Bounce Time of DMG OVP	t_{d_DOVP}		-	5	-	cycles
DMG UVP Threshold	V_{DMG_UVP}		0.51	0.55	0.59	V
DMG UVP Debounce Time	t_{d_DUVP}			6		Ms
DMG Pin Current	I_{DMG}	CS limit is 0.6V		350		μA
		CS limit is 0.8V		340		μA
GATE Section						
Output Low Level	V_{OL}		-	-	1	V
Output High Level	V_{OH}		7	-	-	V
Rising time	t_R	V_{DD}=20V, GATE=1nF, Time when GATE pin voltage rises from 0V to 9V.		90	180	ns
Falling time	t_F	V_{DD}=20V, GATE=1nF, Time when GATE pin voltage drops from 90% to 10%.		35	60	ns
Output source current	I_{SOURCE}	GATE=33nF		350		mA
Output sink current	I_{SINK}	GATE=33nF		550		mA
Output clamp voltage	V_{O_CLAMP}	VCC=20V, GATE=1nF	10	12	14	V
Minimum OUT voltage	V_{O_MIN}	V^{DD}= V_{CC_OFF}+0.5V, GATE=1nF	7.0			V
Thermal Section						
Internal OTP threshold	T_{OTR}		130	145	-	℃
OTP Shutdown Hysteresis	T_{OTR_HYST}		-	20	-	℃

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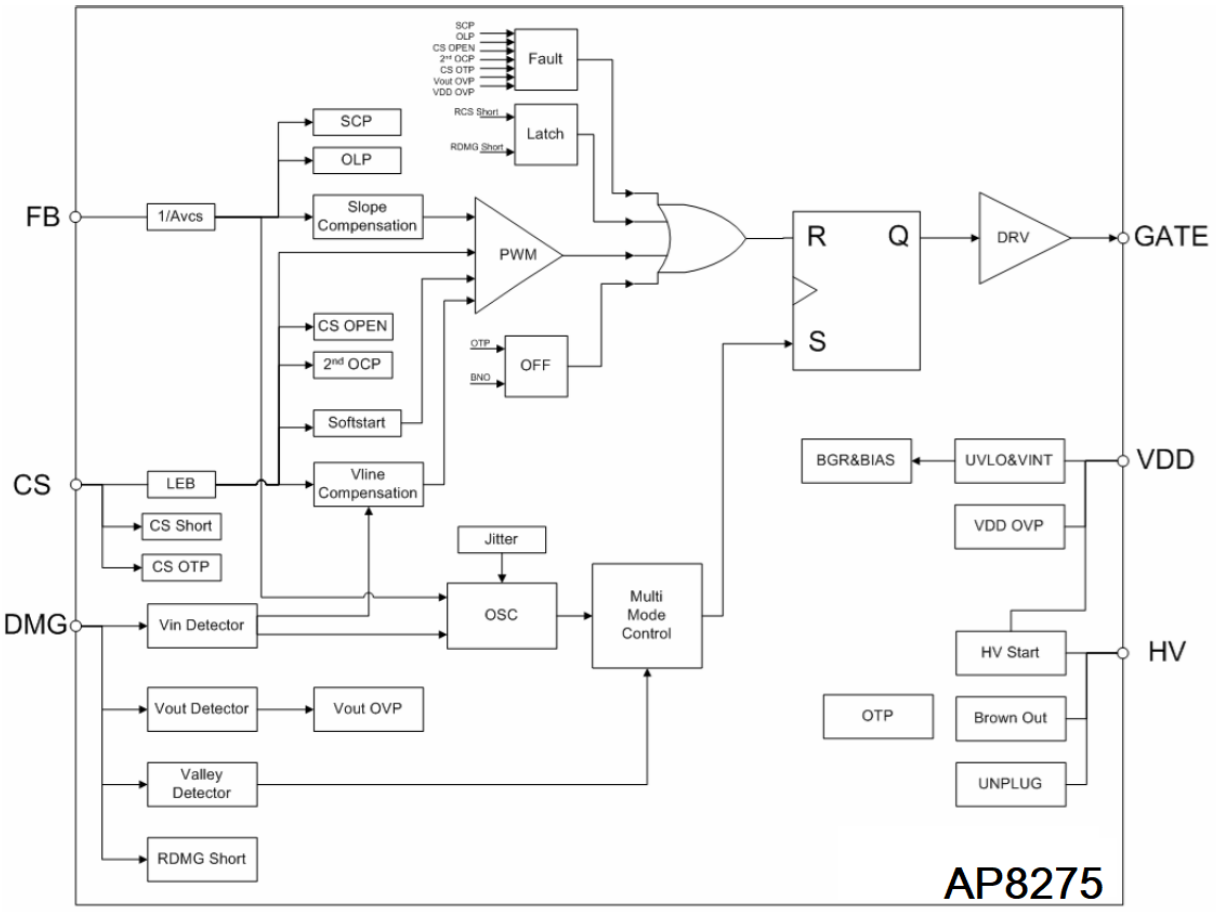
BLOCK DIAGRAM



DETAILED INFORMATION

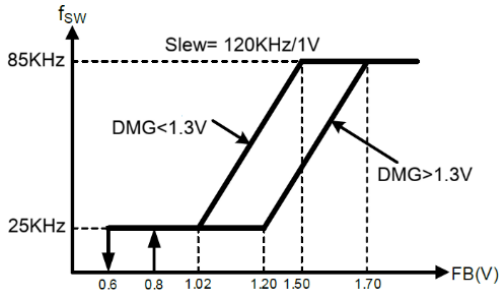
Startup

At start up, the internal high-voltage current source supplies the internal bias and charges the external V_{DD} capacitor. When V_{DD} reaches V_{DD_on}, the device starts switching and the internal high-voltage current source stops charging the capacitor. After starting up, the bias is supplied from the auxiliary transformer winding.

Operation Mode

The AP8275 adopts a CCM and valley switching multi-mode control scheme to optimize system efficiency across different load conditions.

Under heavy load, the controller operates in continuous conduction mode (CCM). As the load decreases and the inductor current transitions into BCM/DCM, the controller enables valley switching, turning on the MOSFET at the valley of the V_{DS} waveform to reduce switching loss and improve efficiency, especially under high-line conditions.



To further enhance efficiency in low output voltage applications, such as 5 V USB PD/PPS systems, the AP8275 implements an alternative FB versus switching frequency (f_{SW}) control curve. When the DMG pin voltage is lower than 1.3 V (with hysteresis), the controller follows the left-hand-side curve, allowing the switching frequency to decrease more aggressively at lower output voltages.

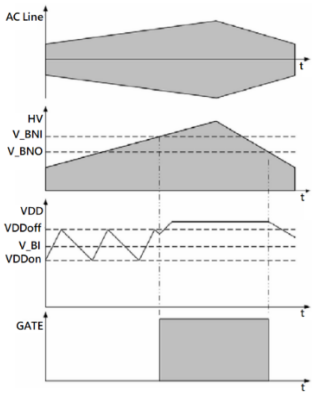
Compared to the conventional right-hand-side curve, this approach reduces the peak and RMS inductor current at the same FB level, thereby improving overall efficiency.

At extremely light load to no-load conditions, switching loss becomes dominant. To address this, the AP8275 integrates burst mode operation. When the FB pin voltage falls below V_{ZD_OFF} (0.6 V), switching stops. The controller resumes operation only when the FB pin voltage rises above V_{ZD_ON} (0.8 V)

Brown-in/out protection

The A8275 features accurate brown-in (BNI) and brown-out (BNO) protection via the HV pin.

When the HV pin voltage exceeds 100 V (BNI threshold), the controller starts operation. When the HV pin voltage falls below 90 V (BNO threshold) for longer than 105 ms (debounce time), the controller stops switching and enters auto-recovery mode.



X-Cap discharge

The AP8275 features an integrated X-capacitor discharge function via the HV pin.

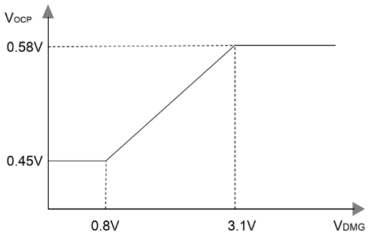
When the AC input is unplugged, the device actively discharges the X-capacitor until the voltage falls within a safe level. This built-in discharge mechanism eliminates the need for an external discharge resistor, thereby reducing input power consumption.

After the AC input is disconnected for more than 47 ms (delay time), the HV pin provides a discharge current of approximately 5 mA. The minimum discharge activation time is 47 ms.

Auto-Tune CS Limited for the Output Range

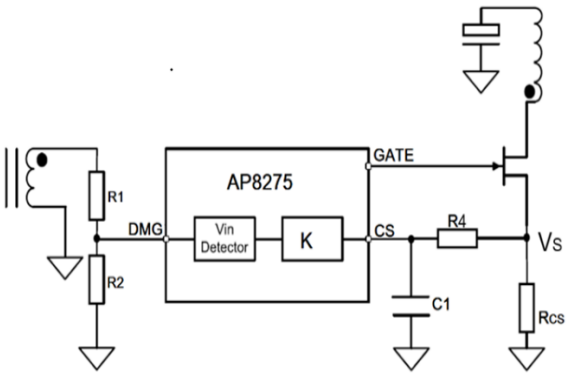
To meet the LPS standard for PD/PPS applications, the OCP threshold is variable as the sampled DMG pin voltage changes.

It is recommended to keep DMG=0.8V for 5V output voltage.



AC Line Input Compensation

The AP8275 offers Line Input Compensation; this feature improves the power limit constant output. The AP8275 detects the input voltage across DMG pin and generates the compensated current. Thus, the compensated current can be calculated as $I_{LC}=K*I_{DMG}$, where K is the compensated coefficient. ILC multiplied R3 equals the compensated voltage that can limit the pulse-by-pulse current. Then the $V_{CS}=[((V_{AC} \times \sqrt{2}/ R1)\times(N_{AUX}/ N_{PRI})) \times 66.7\% \times R4] + V_S$



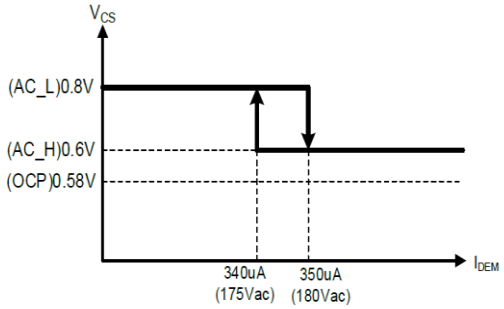
Internal Sloe Compensation

For peak current mode control, sub-harmonic oscillation may occur when the duty cycle exceeds 50%. By introducing a compensation ramp equal to the downslope of the inductor current, this oscillation can be effectively damped within one switching cycle. The AP8275 integrates slope compensation ranging from 0 mV to 300 mV, covering a duty cycle from 0% to the maximum duty cycle (DMAX).

CS Pin Hard Limit Levels for Peak Load

To prevent transformer saturation at peak load, the AP8275 implements two hard current-limit thresholds at 0.6V and 0.8V, both higher than the OCP threshold of 0.58V, to support peak load conditions.

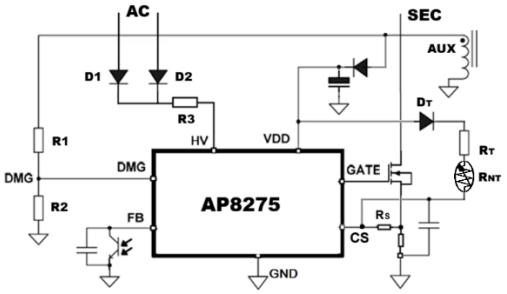
The CS hard limit is set to 0.8V under low AC input conditions when the DMG source current (IDMG) is less than 340 μA. When the DMG source current (IDMG) exceeds 350 μA, the CS hard limit is reduced to 0.6V. An IDMG greater than 350 μA, corresponding to approximately 180 VAC input, is recommended.



Programmable DMG OVP/UVP

In the AP8275, output over-voltage protection (OVP) is implemented by sampling the DMG pin voltage during the gate-off period. This sampled signal is compared with the internal OVP threshold (4V) to determine whether the output voltage has reached a dangerous level.

The OVP threshold can be set according to the following equation:



$$V_{OVP} = \frac{R_2 + R_1}{R_2} \times V_{DEM\_OVP} \times \frac{N_{SEC}}{N_{AUX}}$$

Where:

- N_{SEC}: Secondary winding turns
- N_{AUX}: Auxiliary winding turns

If the DMG pin voltage drops below 0.55V, the AP8275 stops switching until the abnormal condition is removed.

The output under-voltage protection (UVP) threshold is calculated as:

$$V_{UVP} = V_{OVP} \times \frac{V_{DEM\_UVP}}{V_{DEM\_OVP}}$$

Programmable External CS OTP

The AP8275 includes an over-temperature protection (OTP) mechanism via the CS pin. With the appropriate external circuit, OTP can be implemented using an NTC thermistor.

By sensing the CS pin voltage during the gate-off period, the temperature at the hotspot (via the NTC) is monitored. If the CS pin voltage exceeds 0.55V (V_{CS_OTP}) for more than 5 switching cycles (debounce time), the gate signal is immediately shut down to prevent overheating.

The OTP threshold is calculated as:

$$V_{CS\_OTP} = V_{AUX} - V_{DOTP} \times \frac{R_S}{R_{NTC} + R_S + R_{DOTP}}$$

Where:

- V_{CS_OTP}: CS OTP threshold
- R_{NTC}: NTC resistance
- R_S, R_{DOTP}: External resistors

Output Short-Circuit Protection (SCP)

When an output short circuit occurs, the energy supplied from the auxiliary winding to regulate the VCC capacitor is significantly reduced, causing the VCC voltage to drop rapidly below the turn-off threshold.

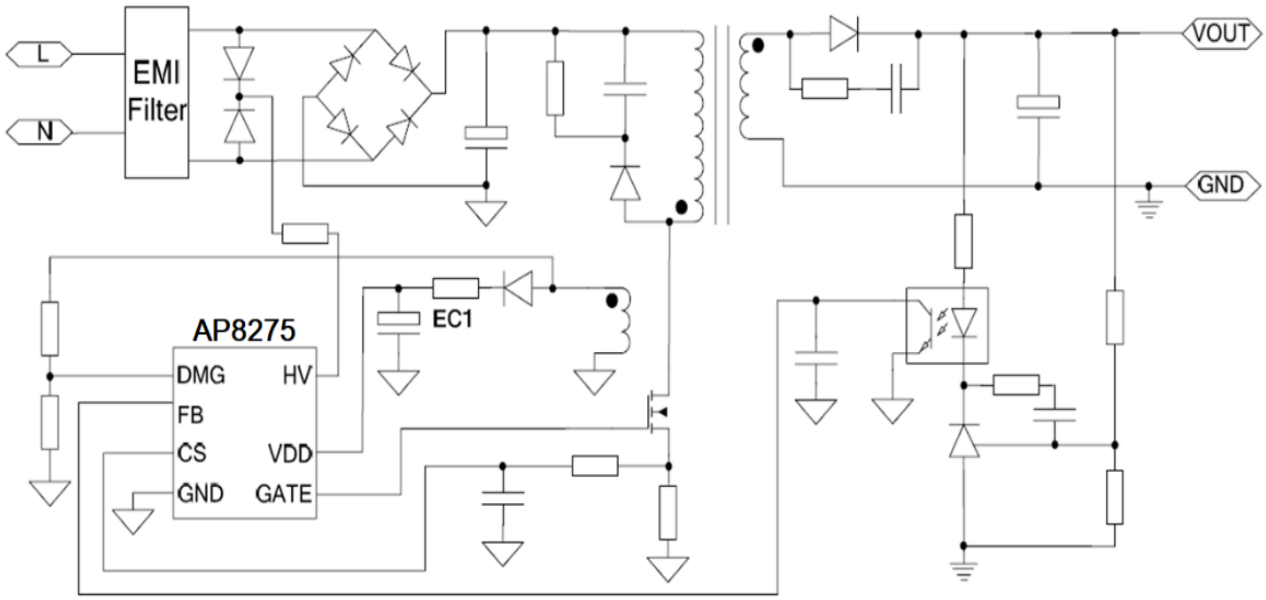
Before the FB OLP and CS OCP mechanisms are triggered, if the CS pin voltage exceeds the OCP threshold for more than 7 consecutive switching cycles, the controller immediately stops switching to provide fast output short-circuit protection.

VCC Self-Recovery Mode

To reduce system power consumption under protection conditions, the AP8275 enters a self-recovery mode. In this mode, the controller will restart only after the VCC voltage drops below the turn-off threshold (9.5V) eight times.

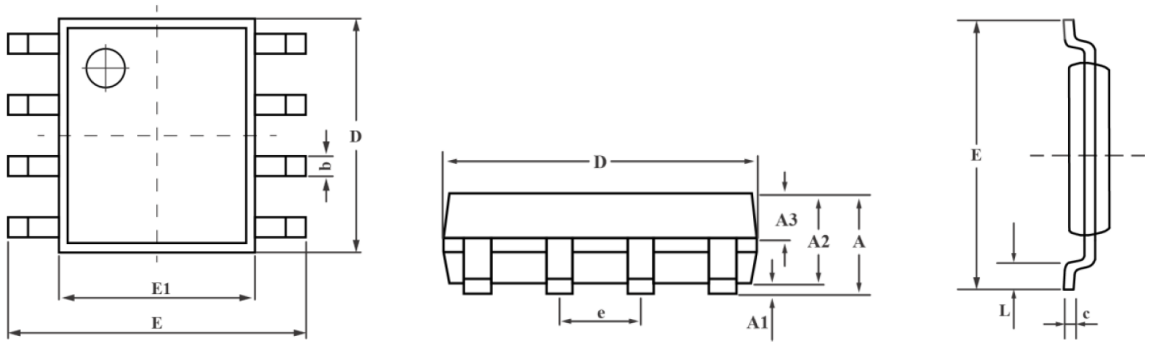
Typical Application

The VDD capacitor (EC1) should be located as close as possible to the VDD and GND pins to ensure optimal performance.



PACKAGE INFORMATION

Dimension in SOP8 (Unit: mm)



Symbol	Min	Max
A	1.35	1.75
A1	0.10	0.25
A2	1.30	1.50
A3	0.55	0.70
b	0.33	0.51
C	0.17	0.25
D	4.70	5.10
E	5.80	6.20
E1	3.80	4.00
e	1.27 BSC	
L	0.4	0.8

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