DESCRIPTION

The A6111 is a high-performance positive low-dropout (LDO) linear regulator designed for applications requiring ultra-low dropout voltage and high power supply ripple rejection (PSRR). The device delivers up to 1 A of continuous output current with an input voltage range of 2.2 V to 6 V. The A6111 employs a P-channel MOSFET pass element to achieve excellent transient response while requiring only a 4.7 µF ceramic output capacitor for stable operation. An external enable (EN) pin allows the regulator to be placed in shutdown mode to reduce power consumption. In addition, a bypass capacitor connected to the NR pin further improves output noise performance, making the device suitable for noise-sensitive analog and RF applications.
The A6111 is available in DFN8 (3×3) package.

APPLICATIONS

- Telecom/Networking Cards
- Motherboards/Peripheral Cards
- Industrial Applications
- Wireless Infrastructures
- Set-Top Boxes
- Medical Equipment's
- Notebook Computers
- Battery Powered Systems

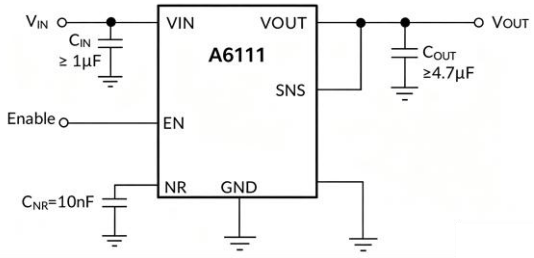
ORDERING INFORMATION

Package Type	Part Number	
DFN8(3x3) SPQ: 5,000pcs/Reel	J8	A6111J8VR
Note	R: Tape & Reel V: Halogen free Package	
AiT provides all RoHS products		

FEATURES

- Input Voltage Range: 2.2V ~ 6V
- Output Voltage Range:
  Fixed Option: 0.8V, 1.0V, 1.2V, 1.8V, 2.5V, 3V, 3.3V and 5.0V
- Up to 1A Load Current
- High PSRR: 66dB at 1kHz, 33dB at 1MHz
- Excellent Noise Immunity
- Very Low Dropout: 175mV Typical at 1A
- Operating Junction Temperature Range: −40°C to +125°C
- Fast Transient Response for Line and Load Variations
- Stable with a 4.7 µ F Output Ceramic Capacitor
- Output Voltage Accuracy: ±3% Over Line, Load, and Temperature Variations
- Enable Control Function
- Over-Current Protection
- Over-Temperature Protection

TYPICAL APPLICATION

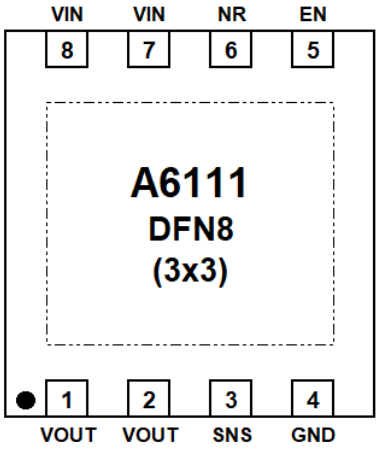


C_{IN} : To improve source voltage noise.

C_{NR} : Noise Reduction Capacitor.

C_{OUT} : A ≥4.7uF ceramic capacitor.

PIN DESCIPTION



DFN8(3x3), J8

Top View

PIN#	Symbol	Function
1, 2	V_{OUT}	Output of the regulator. Decouple this pin to GND with at least 4.7μF for stability.
3	SNS	Output Voltage Sense Input Pin (fixed voltage version only). Connect this pin to the load side of the output trace only in the fixed voltage version
4, 9(Exposed Pad)	GND	System ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
5	EN	Enable control input. Connecting this pin to logic high enables the regulator or driving this pin low puts it into shutdown mode. EN can be connected to IN if not used. (EN pin is not allowed to be left floating.)
6	NR	Noise reduction input. Decouple this pin to GND with an external capacitor can not only reduce output noise to very low levels but also slow down the VOUT rise like a soft start behavior.
7, 8	V_{IN}	Supply input. A minimum of 1μF ceramic capacitor should be placed as close as possible to this pin for better noise rejection.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

V_{IN}, Input voltage		-0.3V ~ +7V
V_{EN}, Enable input voltage		-0.3V ~+7V
I_{OUT}, Current		Internally limited
$R_{\theta JA}$, Package thermal impedance (1)	DFN8(3x3)	53°C/W
T_J, Junction Temperature (2)		-40℃ ~ +150℃
T_{STG}, Storage Temperature Range		-65℃ ~ +150℃
$V_{(ESD)}$ Electrostatic discharge	Human-Body Model (HBM), ANSI/ESDA/JEDEC JS001-2024	±2000V
	Charge Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1000V

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(1) $R_{\theta JA}$ is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. $R_{\theta JC}$ is measured at the exposed pad of the package.

(2) The maximum power dissipation is a function of TJ(MAX), $R_{\theta JA}$, and TA. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB.

RECOMMENDED OPERATING CONDITIONS

T_A = 25°C (Room Temperature), unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}, Input Voltage Range	-	2.2	-	6	V
V_{OUT}, Output Voltage	-	0.8	-	5.0	V
I_{OUT}, Output Current Range on I_{OUT}	-	0	-	1000	mA
C_{OUT}, Output Capacitor	-	4.7	-	100	μF
C_{NR}, Noise Reduction Capacitor	-	1	-	100	nF
T_J, Junction Temperature	-	-40	-	125	ºC

ELECTRICAL CHARACTERISTICS

Over operating temperature range (–40°C ≤ T_J ≤ 125°C), V_{IN}=$V_{OUT(nom)}$+0.5V or 2.2V, V_{OUT} = 0.8V and 5.5V, I_{OUT} = 1mA, V_{EN} = 2.2V, C_{NR} = 10nF, C_{OUT} = 4.7µF, (unless otherwise noted); typical values are at T_J=25°C.

Parameter	Symbol	Conditions		Min. (2)	Typ. (2)	Max. (2)	Unit
POWER SUPPLY AND CURRENTS							
Input Voltage (1)	V_{IN}	-		2.20	-	6	V
Under Voltage Lockout	UVLO	V_{IN} rising		-	2.10	-	V
Hysteresis	V_{HYS}	V_{IN} falling		-	200	-	mV
Quiescent Current	I_Q	I_{OUT} = 0mA, V_{EN} = 1.2V		-	125	-	µA
Ground Pin Current	I_{GND}	I_{OUT} = 1A, V_{OUT} = 3.3V, V_{EN} = 1.2V		-	1	-	mA
Shutdown Current	I_{SD}	V_{EN} = 0V, V_{IN} = 6V		-	0.01	1	µA
OUTPUT VOLTAGE							
Output Voltage Range	V_{OUT}	-		0.80	-	5.50	V
DC Output Accuracy (1)	ΔV_{OUT}	V_{IN} = $V_{OUT\ (nom)}$+0.5V to 5V, I_{OUT} =1mA to 500mA		-	±2	-	%
		V_{IN} = $V_{OUT\ (nom)}$+0.5V to 6V, I_{OUT} =1mA to 1A		-	±3	-	
Line Regulation (1)	$\Delta V_{OUT(\Delta VIN)}$	V_{IN} = V_{OUT} + 0.5V to 6V, I_{OUT} = 1mA		-	0.20	-	%/V
Load Regulation (1)	$\Delta V_{OUT(\Delta IOUT)}$	V_{IN} =V_{OUT} +0.5V, I_{OUT} = 1mA to 1A		-	20	-	mV
Output Voltage Temperature Coefficient (4)	$\frac{\Delta V_{OUT}}{\Delta T_A \times V_{OUT}}$	T_J = -40°C ~+85°C, I_{OUT} = 1mA		-	80	-	ppm/°C
		T_J = -40°C ~+125°C, I_{OUT} = 1mA		-	70	-	
Maximum Output Current (5)	I_{OUTMAX}	-		1	-	-	A
DROPOUT VOLTAGE-							
Dropout Voltage (6)	V_{DO}	I_{OUT} = 1A	V_{OUT}=3.3V	-	230	-	mV
			V_{OUT}=5V	-	175	-	
POWER SUPPLY REJECTION RATIO AND NOISE							
Power Supply Rejection Ratio (7)	PSRR	V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 100mA, C_{NR} = 10nF	f = 100Hz	-	65	-	dB
			f = 1kHz	-	66	-	
			f = 10kHz	-	49	-	
			f = 100kHz	-	40	-	
			f = 1MHz	-	33	-	

Parameter	Symbol	Conditions		Min. (2)	Typ. (2)	Max. (2)	Unit
Output Noise Voltage (7)	V_N	BW= 10Hz~ 100kHz, V_{IN} = 4.3V, V_{OUT} = 3.3V, I_{OUT} = 100mA	C_{NR} = 1nF	-	70	-	μV_{RMS}
			C_{NR} = 10nF	-	37	-	
			C_{NR} = 100nF	-	30	-	
ENABLE AND STARTUP TIME							
Enable High(enabled)	V_{IH}	V_{IN} = 2.2V to 6V, EN rising		1.2	-	-	V
Enable Low(shutdown)	V_{IL}	V_{IN} = 2.2V to 6V, EN falling		-	-	0.4	V
Enable Pin Current, Enabled	I_{EN}	V_{IN}=6V, V_{EN}=0V		-	-	1	µA
		V_{IN}=6V, V_{EN}=6V		-	0.03	1	
Startup Time (3)	t_{STR}	V_{OUT}=3.3V, I_{OUT}=10mA, C_{OUT} = 4.7µF	C_{NR} = 1nF	-	95	-	µs
			C_{NR} = 10nF	-	910	-	
Output discharge FET R_{DS-ON}	R_{DIS}	V_{IN}=5V, V_{EN}<V_{IL} (output disable)		-	300	-	Ω
PROTECTIONS							
Output Current Limit	I_{LIM}	V_{OUT} = 0.85 × V_{OUT}		-	1300	-	mA
Thermal Shutdown Temperature (7)	T_{SD}	Shutdown, temperature increasing		-	155	-	°C
		Reset, temperature decreasing		-	135	-	°C

(1) Minimum VIN = V_{OUT} + V_{DO} or 2.2V, whichever is greater.
(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method. 135°C
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(4) Output voltage temperature coefficient is defined as the worst-case voltage change divided by the total temperature range.
(5) Maximum output current is affected by the PCB layout, size of metal trace, the thermal conduction path between metal layers, ambient temperature and the other environment factors of system. Attention should be paid to the dropout voltage when V_{IN} < V_{OUT} + V_{DROP}.
(6) The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 2% below the value of V_{OUT} for V_{IN} = V_{OUT} nom+ 0.5V
(7) Guaranteed by design and characterization, not a FT item

TYPICAL PERFORMANCE CHARACTERISTICS

Fig 1. Quiescent Current vs. Input Voltage

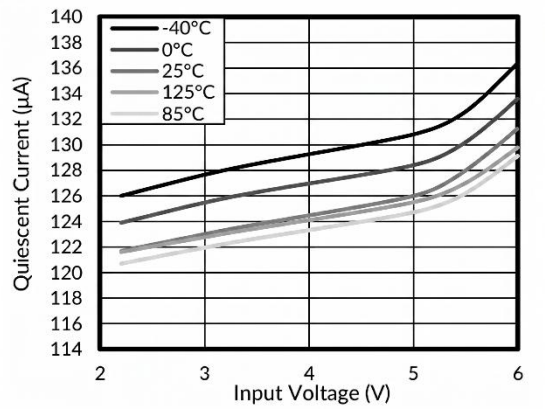


Fig 2. Quiescent Current vs. Temperature

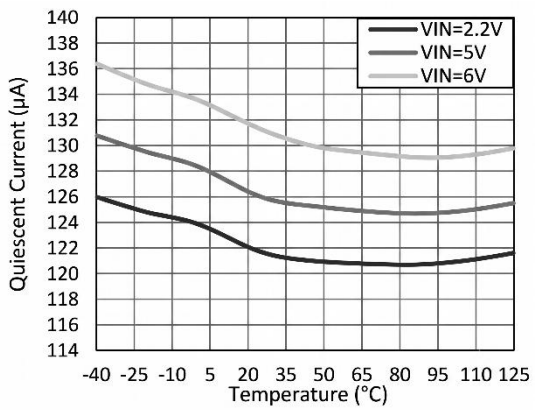


Fig 3. Ground Pin Current vs. Output Current

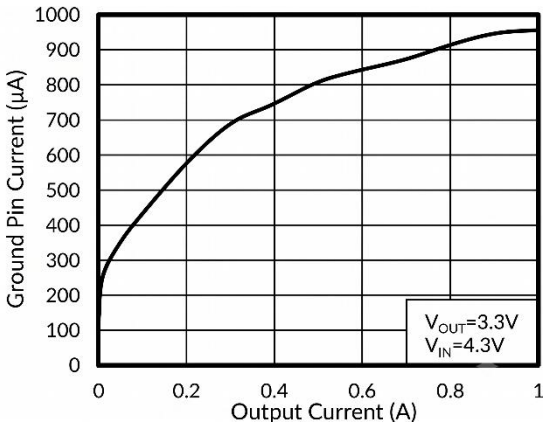


Fig 4. Supply Current vs. Input Voltage

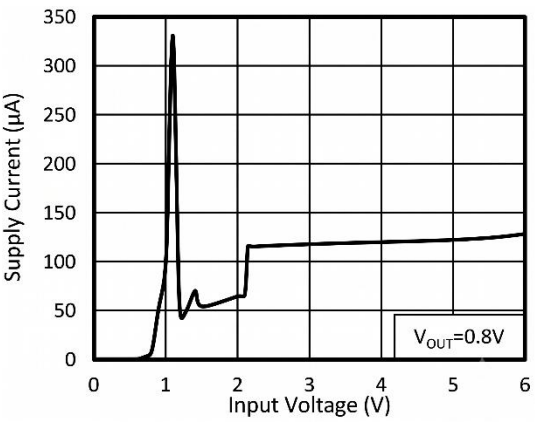


Fig 5. Shutdown Current vs. Temperature

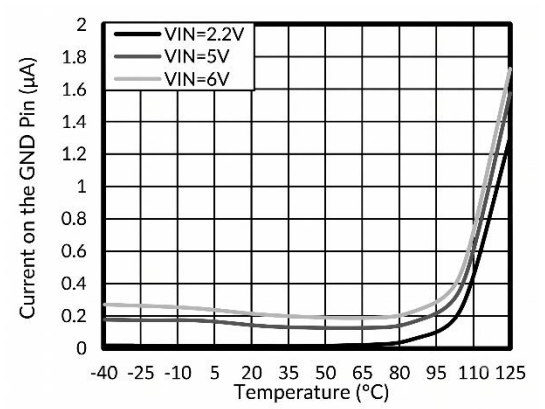


Fig 6. Load Regulation

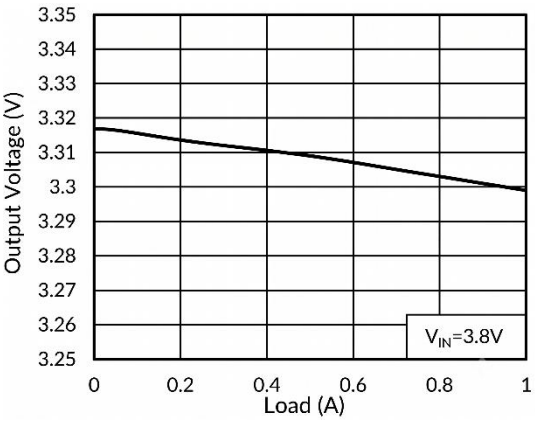


Fig 7. Line Regulation

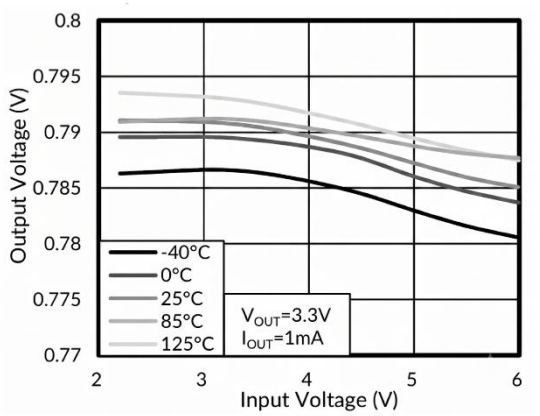


Fig 8. Feedback Voltage vs. Junction Temperature

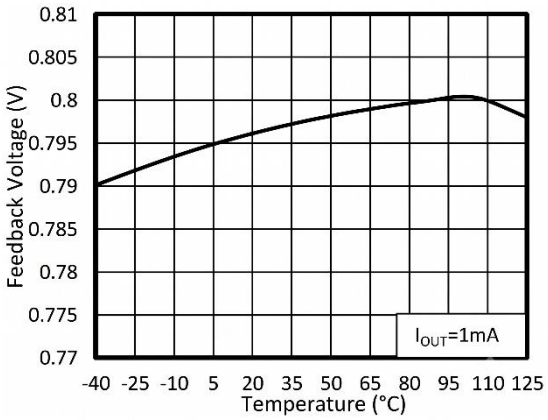


Fig 9. Feedback Pin Current vs. Junction Temperature

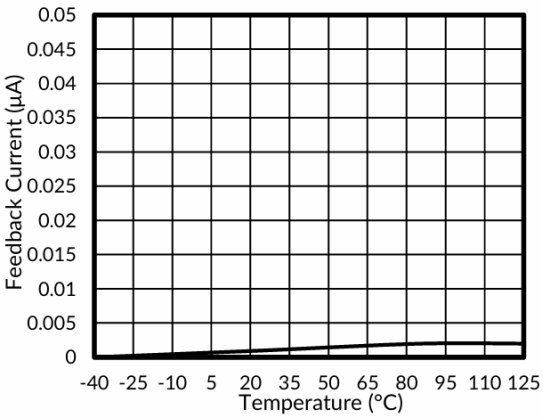


Fig 10. UVLO vs. Junction Temperature

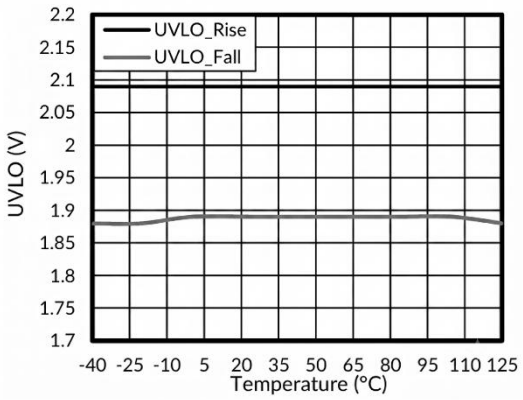


Fig 11. Enable Threshold vs. Input Voltage

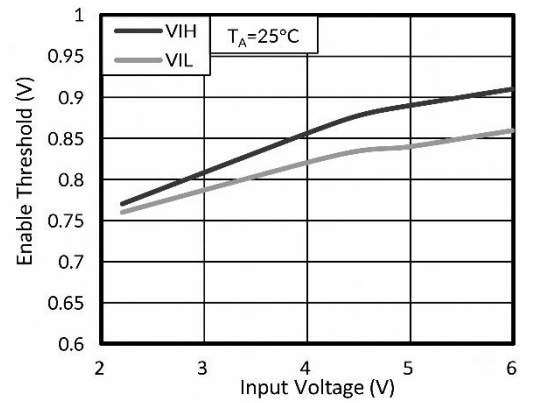


Fig 12. Enable Threshold vs. Junction Temperature

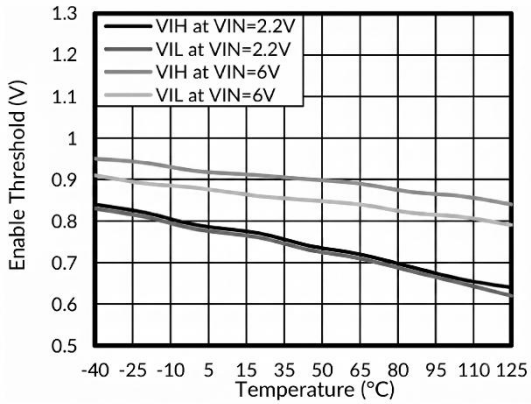


Fig 13. Dropout Voltage vs. Output Current

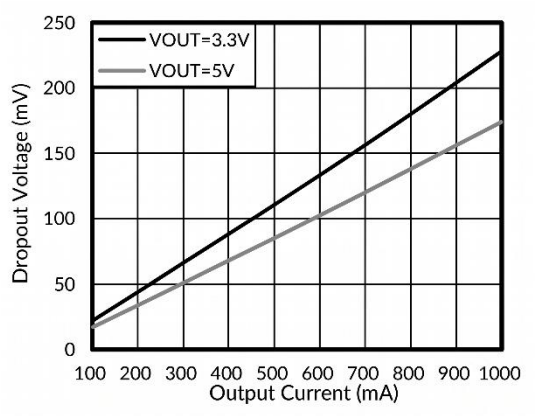


Fig 14. Dropout Voltage vs. Output Current

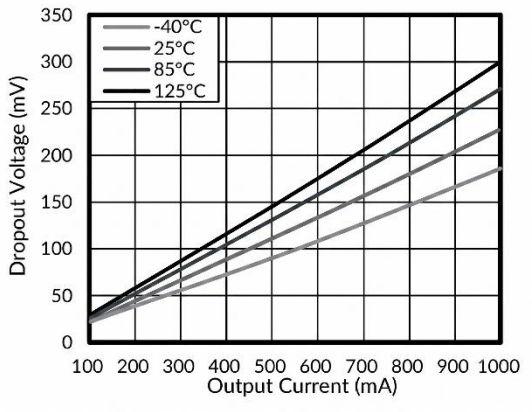


Fig 15. Power Supply Rejection Ratio vs. Frequency

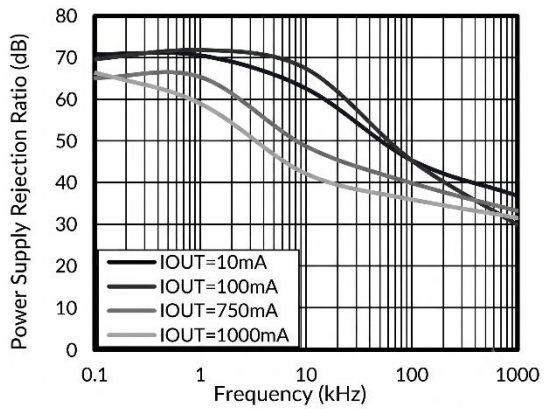


Fig 16. RMS Noise vs. CNR

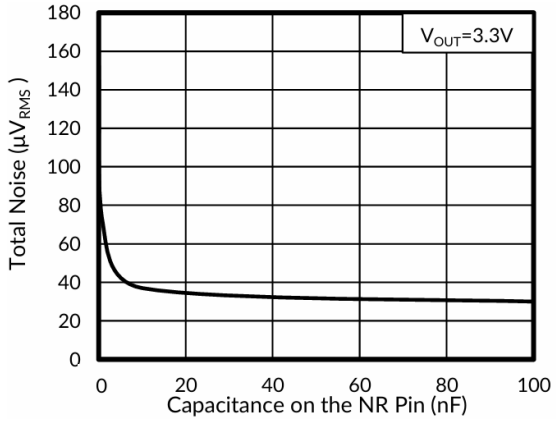


Fig 17. Output Current Limit vs. Temperature

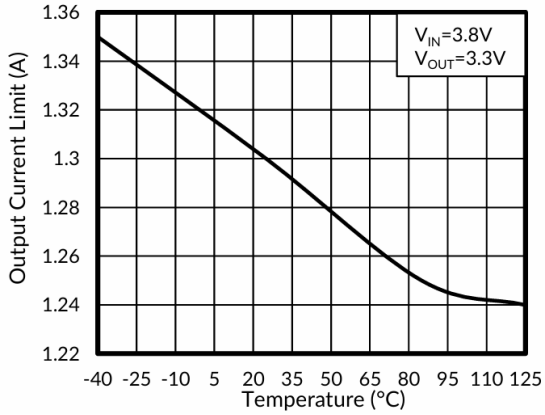


Fig 18. Power On

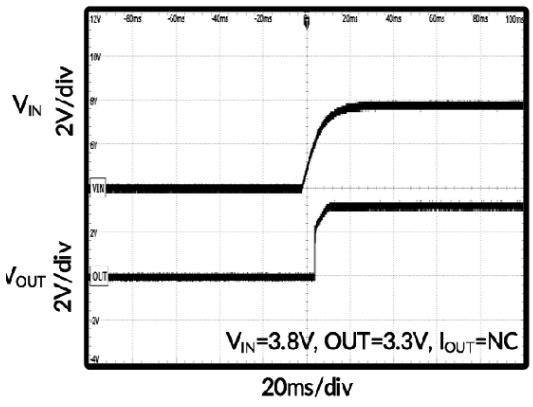


Fig 19. Power Off

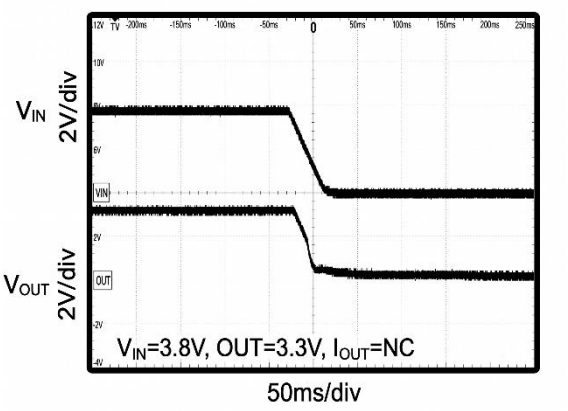


Fig 20. Power On

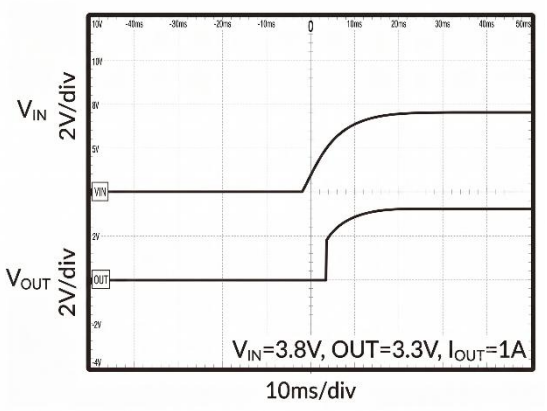


Fig 21. Power Off

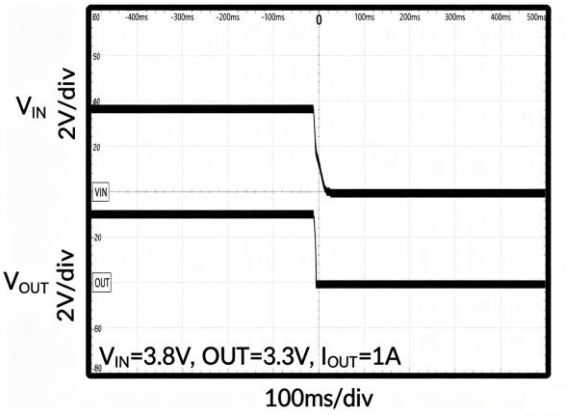


Fig 22. Turn On

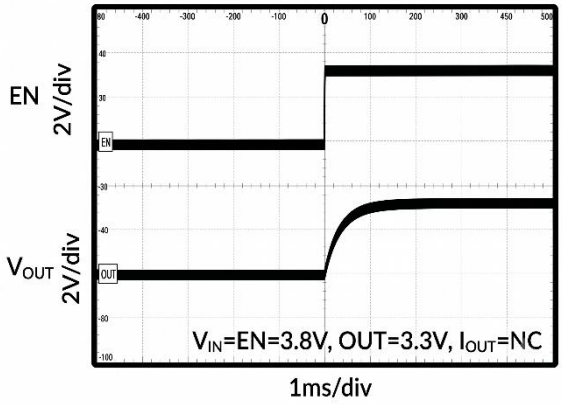


Fig 23. Power Off

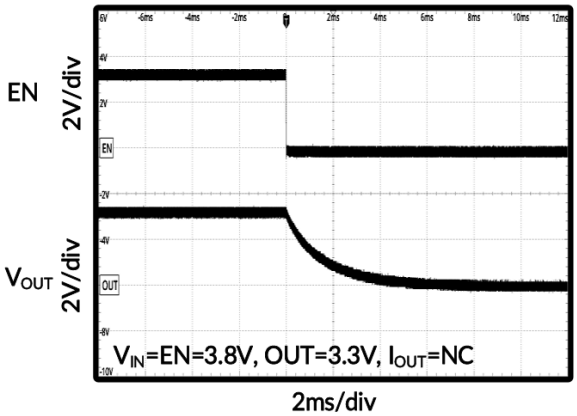


Fig 24. Turn On

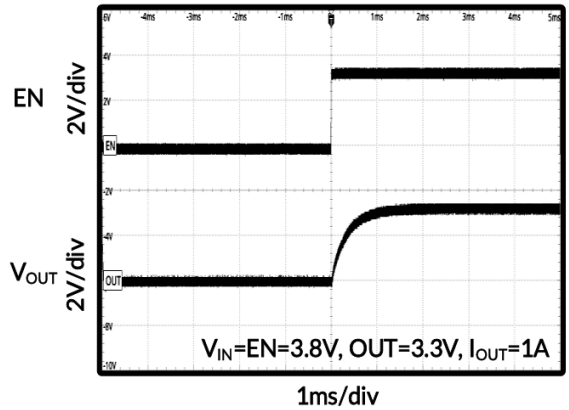


Fig 25. Turn Off

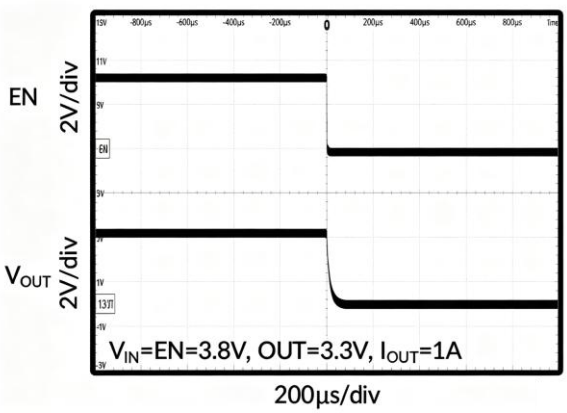


Fig 26. Line Transient Response

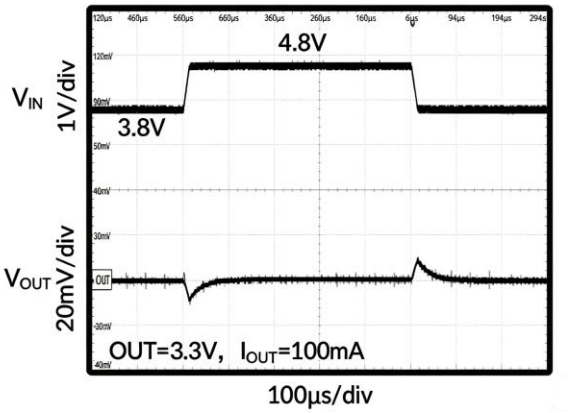


Fig 27. Load Transient Response

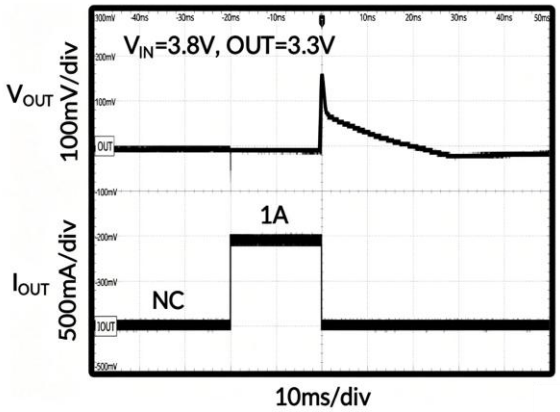


Fig 28. Load Transient Response

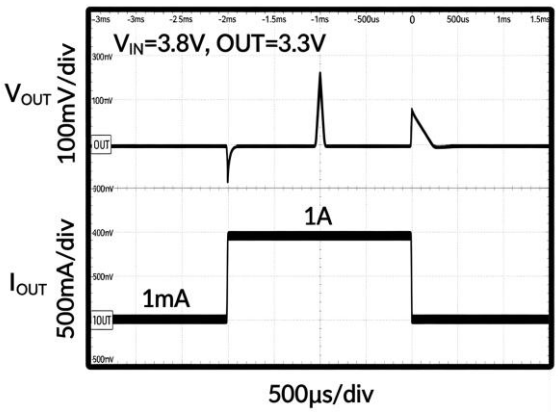
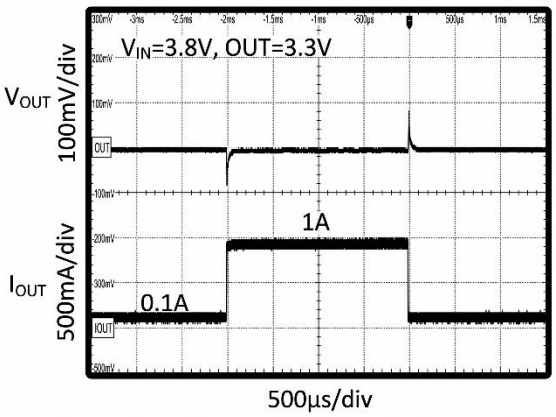
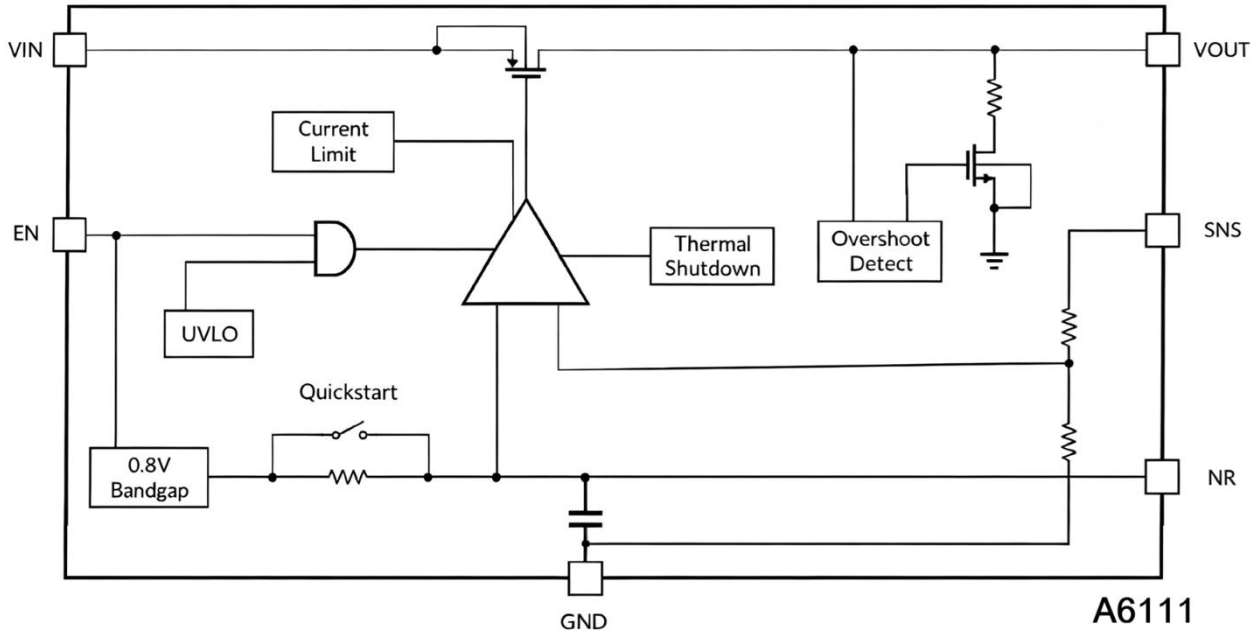


Fig 29. Load Transient Response



BLOCK DIAGRAM



FEATURE DESCRIPTION

The A6111 is a high-performance positive low-dropout (LDO) linear regulator designed for applications requiring low dropout voltage, high output current, and high power supply ripple rejection (PSRR). The device operates from an input voltage range of 2.2 V to 5.0 V and provides up to 1 A of continuous output current.

The A6111 employs a P-channel MOSFET pass element to achieve excellent line and load transient response while requiring only a 4.7 µF ceramic output capacitor for stable operation. An external enable (EN) pin allows the device to enter a low-power shutdown mode, reducing power consumption. In addition, a bypass capacitor connected to the NR pin further reduces output noise, making the A6111 well suited for noise-sensitive analog and portable applications.

Undervoltage Lockout (UVLO)

The A6111 uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly.

Shutdown

The enable pin (EN) is active high and is compatible with standard and low-voltage TTL-CMOS levels. When shutdown capability is not required, the EN pin can be connected to the V_{IN} pin.

Thermal Overload Protection (TSD)

Thermal shutdown disables the output when the junction temperature rises to approximately 155°C which allows the device to cool. When the junction temperature cools to approximately 135°C, the output circuitry enables

Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The thermal shutdown circuitry of the A6111 has been designed to protect against temporary thermal overload conditions. The TSD circuitry was not intended to replace proper heat-sinking. Continuously running the A6111 device into thermal shutdown may degrade device reliability.

Disabled

The regulator is disabled under any of the following conditions:

The input voltage is less than the UVLO threshold minus V_{HYS}, or has not yet exceeded the UVLO threshold.

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising
- threshold. When disenabled, the pull-down device behaves like a 300Ω resistor to ground.
- The device junction temperature is greater than the thermal shutdown temperature.

Internal Current-Limit

The A6111 internal current-limit helps protect the regulator during fault conditions. During current-limit, the output sources a fixed amount of current that is largely independent of the output voltage. For reliable operation, do not operate the device in current-limit for extended periods of time. The A6111 has a built-in body diode that conducts current when the voltage at the V_{OUT} pin exceeds the voltage at the V_{IN} pin. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting can be appropriate.

Startup and Noise Reduction Capacitor

The A6111 incorporates a quick-start circuit to rapidly charge the noise reduction capacitor (C_{NR}) during startup. This architecture enables both fast startup and ultra-low output noise performance. The NR pin is a high-impedance node; therefore, a low-leakage capacitor should be used for C_{NR}. Most ceramic capacitors are suitable for this application. For optimum performance, especially in applications subject to wide temperature variations, a high-quality C0G (NP0) ceramic capacitor is recommended.

A 10nF C0G (NP0) ceramic capacitor is recommended for C_{NR} in most applications to achieve the best startup and output noise performance.

Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, a minimum 1μF low-ESR ceramic capacitor is recommended between the IN and GND pins, placed as close to the device as possible. This capacitor helps suppress input supply disturbances, improves line transient response, and enhances PSRR performance.
A larger input capacitor may be required if the power source is located several inches from the device or if the application experiences large and fast transient loads. The A6111 is designed to be stable with a standard ceramic output capacitor of 4.7μF or greater. X5R or X7R dielectric ceramic capacitors are recommended because they exhibit minimal capacitance and ESR variation over temperature, ensuring stable operation and optimum transient performance.

POWER SUPPLY RECOMMENDATIONS

The device is designed to operate from an input voltage supply range of 2.2V to 6V. The input voltage must provide sufficient headroom to allow the device to maintain a regulated output voltage. The input supply should be well regulated. If the input supply is noisy, adding additional low-ESR input capacitors can help reduce output noise.

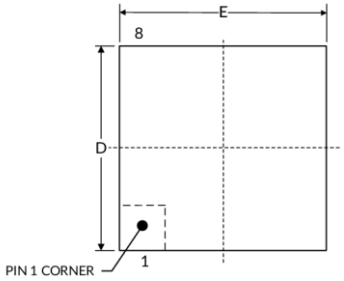
LAYOUT

For best overall performance, place all circuit components on the same side of the PCB and as close as possible to the corresponding LDO pin connections. The ground return connections of the input capacitor, output capacitor, and LDO ground pin should be placed as close to each other as possible and connected using a wide copper area on the component side of the PCB.
The use of vias and long traces for LDO component connections is strongly discouraged, as they introduce additional parasitic inductance and may negatively impact system performance. This grounding and layout scheme minimizes inductive parasitic, reduces load-current transient effects, minimizes noise, and improves overall circuit stability.

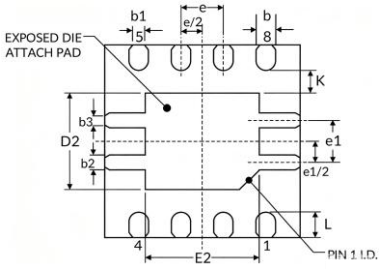
A ground reference plane is also recommended. The ground plane can be embedded within the PCB or placed on the bottom layer of the PCB opposite the component side. This reference plane helps maintain output voltage accuracy, provides noise shielding for the LDO, and acts as a thermal plane to distribute (or dissipate) heat from the LDO device when connected to the exposed thermal pad. In most applications, this ground plane is required to satisfy thermal performance requirements.
To improve AC performance, such as PSRR, output noise, and transient response, it is recommended to design the PCB with separate ground planes for V_{IN} and V_{OUT}, with the two ground planes connected only at the LDO GND pin. In addition, the ground connection of the bypass capacitor must be connected directly to the device GND pin.

PACKAGE INFORMATION

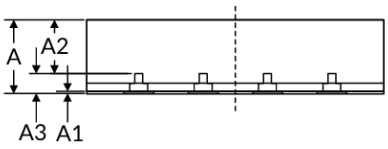
Dimension in DFN8(3x3) (Unit: mm)



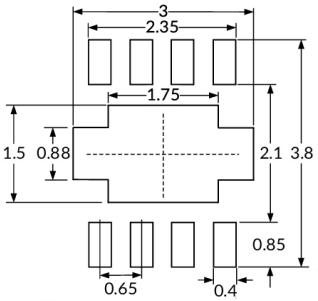
Top View



Bottom View



Side View



RECOMMENDED LAND PATTERN

Symbol	Min.	Max.
A (1)	0.700	0.800
A1	0.000	0.050
A2	0.550 NOM	
A3	0.203 REF. (2)	
b	0.250	0.350
b1	0.180 REF.	
b2	0.180	0.280
b3	0.150 REF.	
D (1)	3.000 BSC. (3)	
D2	1.400	1.600
E (1)	3.000 BSC. (3)	
E2	1.650	1.850
e	0.650 BSC. (3)	
e1	0.650 BSC. (3)	
L	0.300	0.500
K	0.350 REF. (2)	

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