DESCRIPTION

The AG27524 is a dual, high-current, low-side gate driver. Each of its two outputs is capable of sourcing and sinking up to 5 A peak current and supports a maximum supply voltage of 20 V. Each channel features dual independent enable inputs that default to the enabled (ON) state when left unconnected. Fast propagation delays, along with fast rise and fall times, make the AG27524 well suited for high-frequency switching applications.

Additionally, the AG27524 provides closely matched internal propagation delays between Channels A and B, making it ideal for applications that require precise timing between dual gate drivers, such as synchronous rectification.

The AG27524 is available in SOP8 package.

APPLICATIONS

- Pulse laser for distance test
- Battery management systems
- DC-DC converters
- Motor controllers
- Power inverters
- Synchronous rectifier circuits

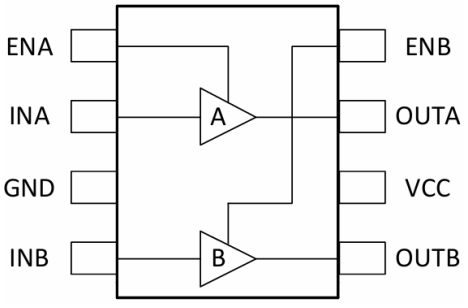
ORDERING INFORMATION

Package Type	Part Number	
SOP8 SPQ: 2,500pcs/Reel	M8	AG27524M8R
		AG27524M8VR
Note	R: Tape & Reel V: Halogen free Package	
AiT provides all RoHS products		

FEATURES

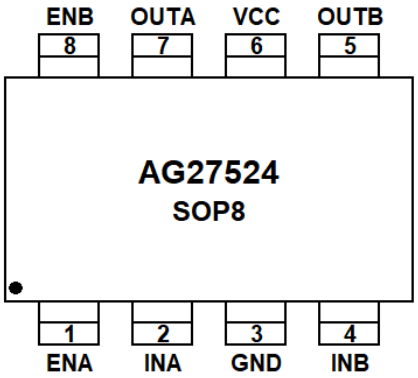
- Dual independent low-side gate drivers, and sourcing and sinking are 5A peak current
- CMOS- and TTL-compatible inputs
- Independent enable input for each channel
- 4.5 V to 20 V operating supply voltage range
- –40°C to +125°C operating junction temperature range
- ±4 kV ESD protection (HBM)
- Thermally enhanced 8-pin SOP package
- Internal undervoltage lockout protection
- Fast input-to-output propagation delay: 15 ns (typ)
- Fast rise and fall times: 7 ns (typ.) with 1.8 nF load
- Matched channel-to-channel propagation delay: 5 ns (max.)

TYPICAL APPLICATION



SOP8

PIN DESCIPTION



SOP8, M8

Top View

PIN#	Symbol	Function
1	ENA	Enable input for Channel A. Logic high enables OUTA; logic low disables OUTA and forces it low. Floating input defaults to logic high through an internal pull-up.
2	INA	Channel A logic input. Internally pulled to GND.
3	GND	Ground. Common ground reference for the device.
4	INB	Channel B logic input. Internally pulled to GND.
5	OUTB	Channel B output, capable of sourcing and sinking 5A
6	V_{CC}	upply voltage.
7	OUTA	Channel A output, capable of sourcing and sinking 5A
8	ENB	Enable input for Channel B. Logic high enables OUTB; logic low disables OUTBand forces it low. Floating input defaults to logic high through an internal pull-up.
Thermal Pad. Connect the thermal pad to GND or leave it floating. Do not connect the thermal pad to any other net. The thermal pad is for heat dissipation only and is not electrically functional..		

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

V_{CC}, DC Supply Power	-0.3V ~ 26V
ENA/ENB pins	-0.3V ~ V_{CC}+0.3V
INA/INB pins	-0.3V ~ V_{CC}+0.3V
OUTA/OUTB pins (pulse <200ns)	-0.2V ~ V_{CC}+0.3V
Junction temperature	-40℃ ~ +125℃
ESD, Susceptibility HBM	±4KV
$R_{\theta JA}$, Package dissipation rating SOP8	190℃/W
T_{STG}, Storage Temperature Range	-55℃ ~ +150℃
T_L, Lead Temperature (Soldering, 10 seconds)	260℃

Stresses above may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
V_{CC} supply voltage	V_{CC}	-	4.5	-	20	V
ENA/ENB/INA/INB	EN/IN	-	-0.3	-	V_{CC}	-
Repetitive Pulse < 200ns	OUT	-	-2	-	V_{CC}	-

ELECTRICAL CHARACTERISTICS

V_{CC}=12V, T_A=25℃, unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply						
Supply Current , V_{CC}=12V	I_{CC}	OUTA and OUTB open	-	1	2.5	mA
V_{CC}=3.0V, INA=INB=V_{CC}	I_{CC_OFF}	-	-	80	120	μA
V_{CC}=3.0V, INA=INB=GND		-	-	60	100	
Under Voltage Lockout (UVLO)						
UVLO rising threshold	$UVLO_{\_ON}$	V_{CC} rising	3.10	3.30	3.50	V
UVLO falling threshold	$UVLO_{\_OFF}$	V_{CC} falling	3.50	3.85	4.20	V
UVLO threshold hysteresis	$UVLO_{\_HYS}$	-	0.20	0.50	0.80	V
Logic inputs (INA, INB, ENA, ENB)						
Input logic low	V_{IN_L}	-	0.90	1.20	1.50	V
Input logic high	V_{IN_H}	-	1.80	2.10	2.40	V
Enable logic low	V_{EN_L}	-	0.85	1.10	1.35	V
Enable logic high	V_{EN_H}	-	1.75	2.05	2.35	V
Input pull up resistor	R_{ENH}	-	-	400k	-	ohm
Input pull down resistor	R_{INL}	-	-	400k	-	ohm
Output drivers (OUTA, OUTB)						
Output pull up resistance	$R_{\_OH}$	I_{OUT}=-10mA, T_J=25℃	-	0.80	1.30	ohm
		I_{OUT}=-10mA	-	1	1.50	
Output pull down resistance	$R_{\_OL}$	I_{OUT}=10mA, T_J=25℃	-	0.60	1.10	ohm
		I_{OUT}=10mA	-	0.80	1.40	
High level output current	$I_{SOUPEAK}$	-	-	5	-	A
Low level output current	$I_{SNKPEAK}$	-	-	-5	-	A
Rise time	T_{RISE}	C_{LOAD}=1.8nF	-	7	15	ns
Fall time	T_{FALL}		-	7	15	ns
Propagation delay, Low to High	T_{DLH}		5	15	25	ns
Propagation delay, High to Low	T_{DHL}		5	15	25	ns
Propagation delay matching	T_{MATCH}		-5	-	5	ns

TYPICAL PERFORMANCE CHARACTERISTICS

Fig 1. Operation Current vs. Frequency

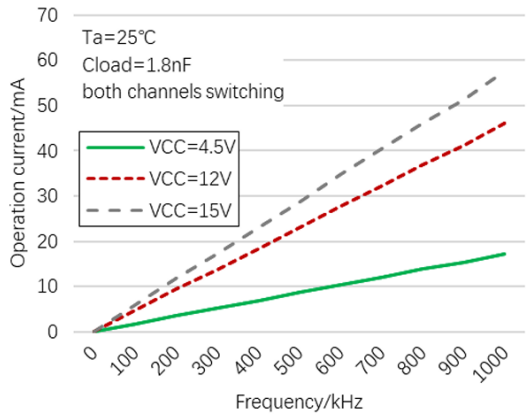
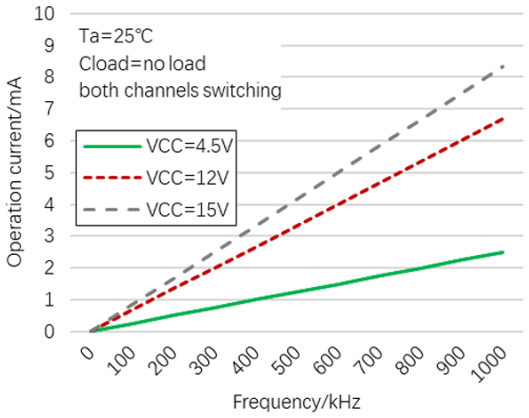


Fig 2. Operation Current vs. Frequency



a

Fig 3. Rise Time vs. V_{CC} Voltage

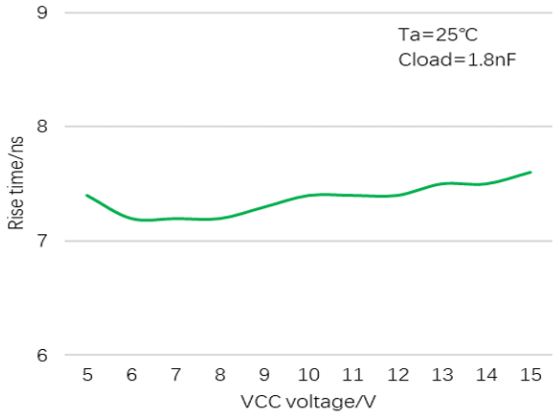


Fig 4. Rise Time vs. V_{CC} Voltage

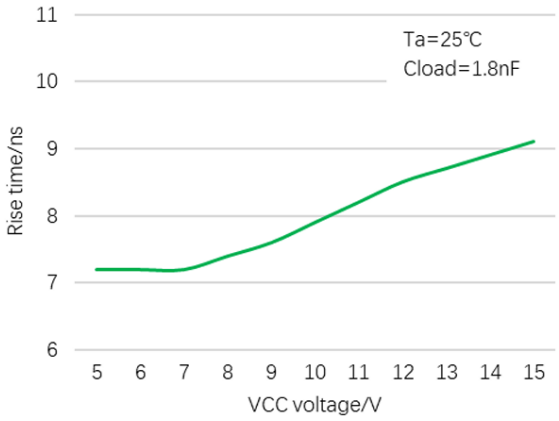


Fig 5. Operation Current vs. Voltage at 100kHz

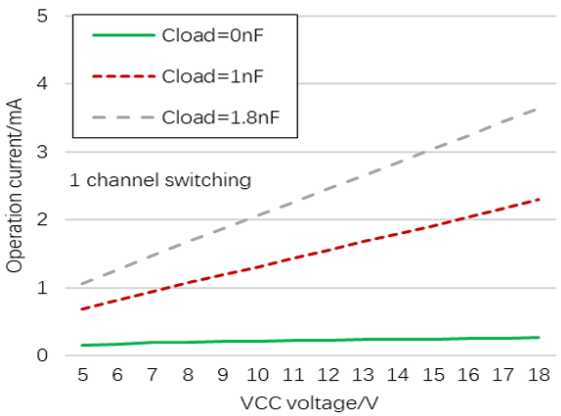


Fig 6. Propagation vs. V_{CC} Voltage

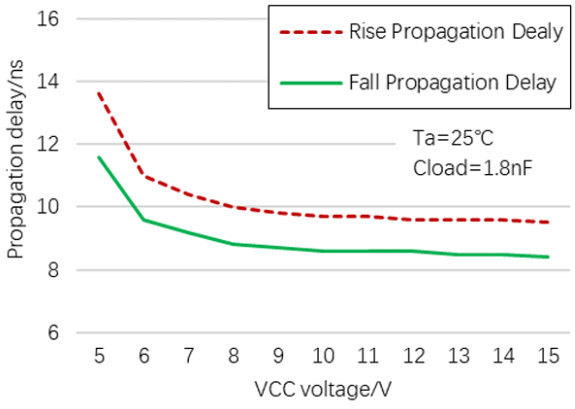


Fig 7. Operation Current vs. Temperature

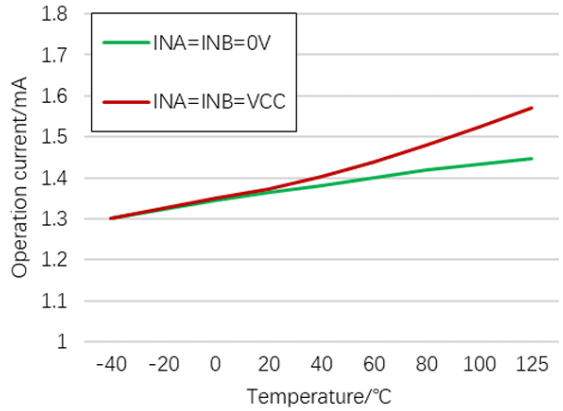
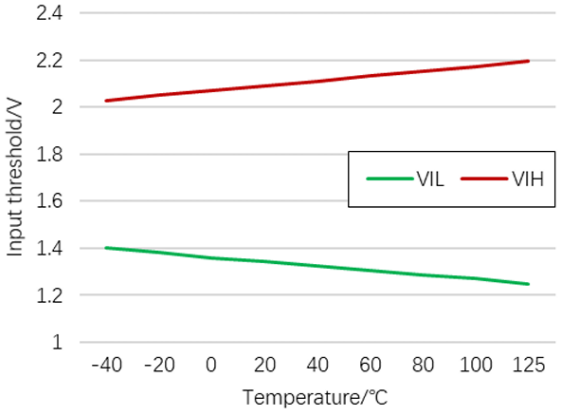
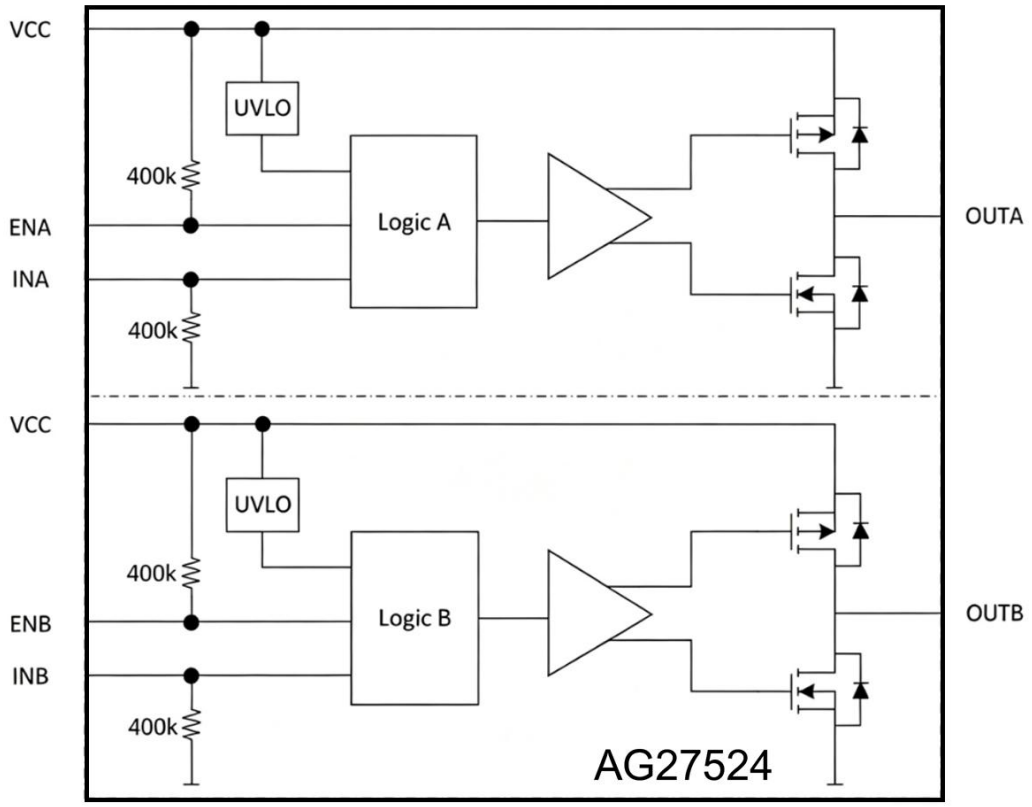


Fig 8. Input Threshold vs. Temperature



BLOCK DIAGRAM



TYPICAL APPLICATION

Fig 1. AG27524 application for one channel

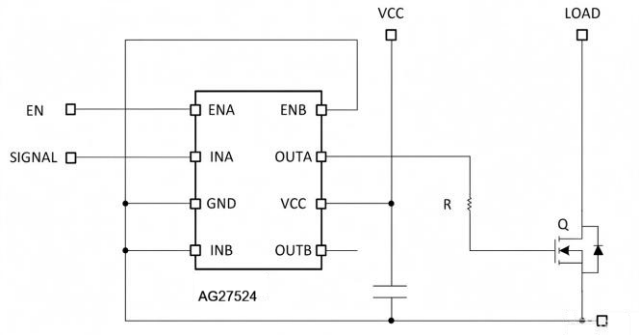


Fig 2. AG27524 application for two channels

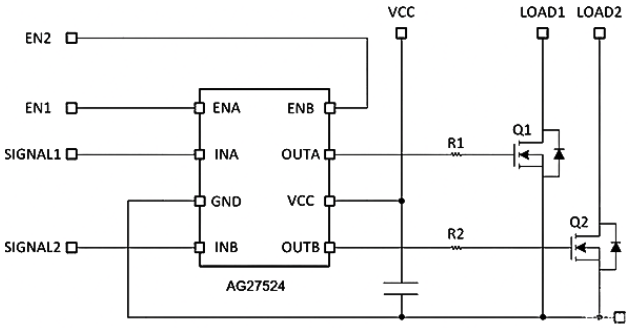


Fig 3. High current forward converter with synchronous rectifier

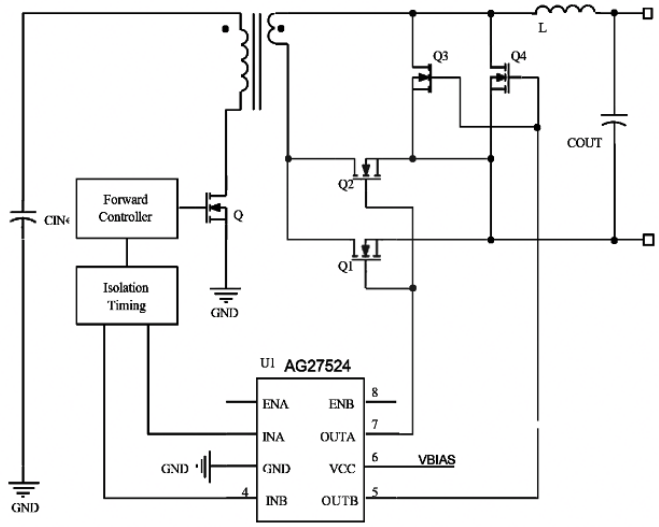


Fig 4. Two brush DC motors driver application

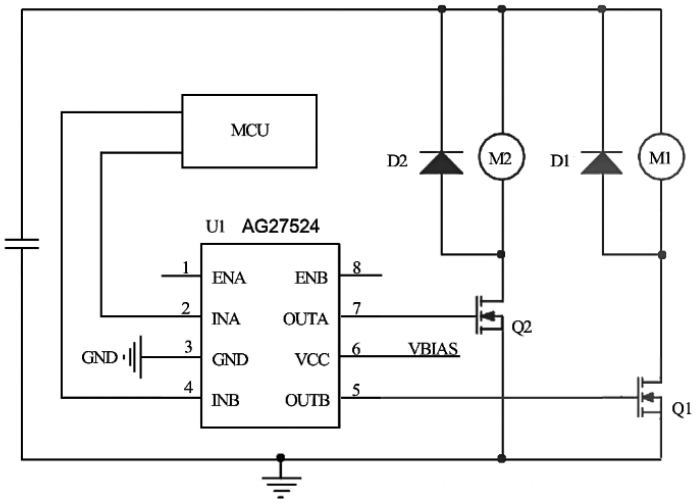
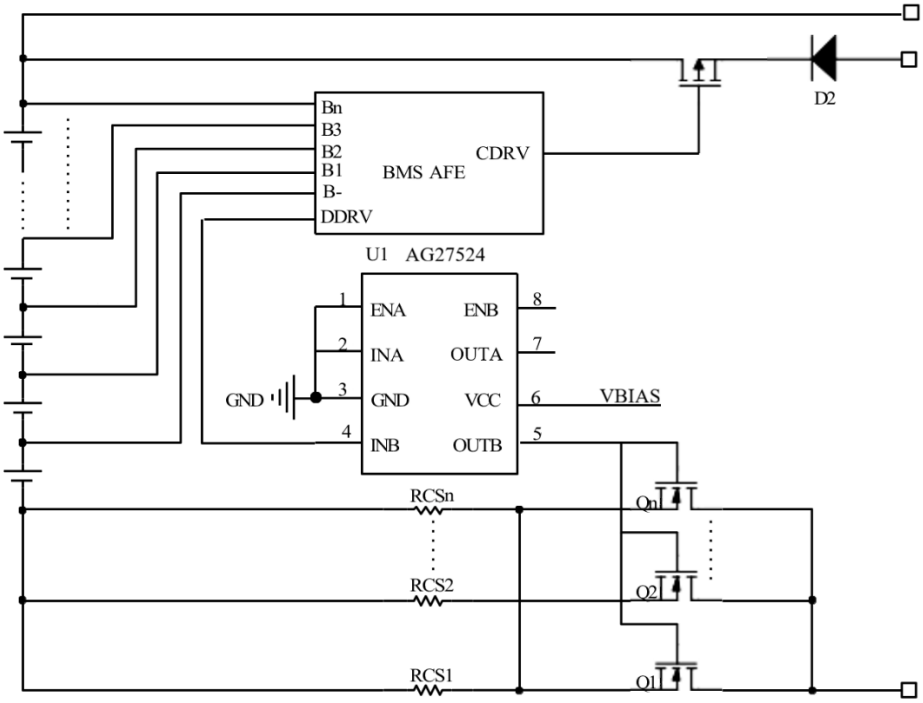


Fig 5. Battery management to drive MOSFETs in parallel

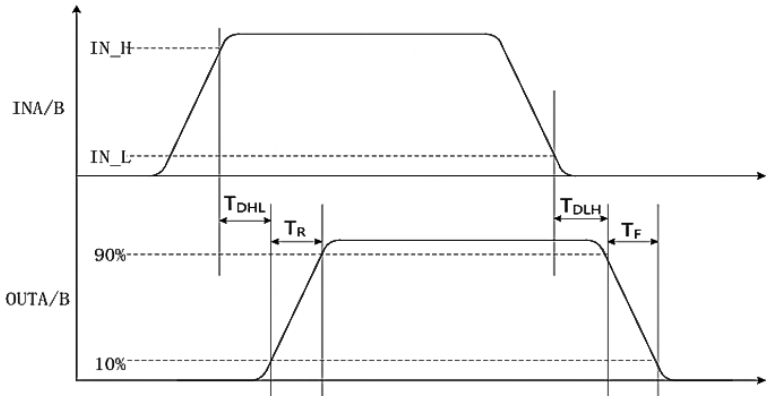


OPERATION DESCRIPTION

Input Threshold

The AG27524 consists of two identical gate driver channels, each capable of operating independently at its rated output current. Channels A and B can be enabled or disabled independently using the ENA and ENB inputs, respectively. The enable inputs feature TTL-compatible input thresholds. If ENA and ENB are left floating, internal pull-up resistors automatically enable both driver channels by default. To increase the output drive capability, Channels A and B may be connected in parallel by tying their corresponding inputs and outputs together. In this configuration, ENA and ENB should also be tied together and driven by the same control signal. When operating the channels in parallel, it is recommended to use a separate gate resistor for each output. Individual gate resistors help limit cross-conduction (shoot-through) current that may occur between the two output stages due to channel-to-channel variations in propagation delay or input threshold.

Fig6. Input INA/B vs. Output OUTA/B timing chart.



Under Voltage Lockout

The AG27524 startup logic is optimized for driving ground-referenced N-channel MOSFETs and incorporates an internal undervoltage lockout (UVLO) function to ensure controlled startup operation. While V_{CC} is rising but remains below the UVLO threshold, the output is held LOW regardless of the states of the input pins. Once the device has exited UVLO and becomes operational, V_{CC} must fall by approximately 0.5 V below the UVLO threshold before the device re-enters the UVLO state and the outputs are disabled. This built-in hysteresis prevents output chatter caused by supply voltage noise during power switching.

The AG27524 is not intended for driving high-side P-channel MOSFETs. During UVLO, the driver output is held low, which can inadvertently turn on a high-side P-channel MOSFET when V_{CC} is below the UVLO threshold

V_{CC} Bypass Capacitor Guidelines

To ensure fast switching performance, a local high-frequency bypass capacitor with low ESR and low ESL should be connected between the V_{CC} and GND pins using the shortest possible PCB traces. This high-frequency bypass capacitor should be used in addition to the 10 µF to 47 µF bulk capacitor typically provided on the driver or controller bias supply. A common design guideline is to select the bypass capacitor value such that the ripple voltage on the V_{CC} supply remains ≤ 5%. This is typically achieved by choosing a capacitance of at least 20 times the equivalent load capacitance, where the equivalent load capacitance is defined as QG / V_{CC}.

Ceramic capacitors in the range of 0.1 µF to 1 µF (or larger) are commonly used. X5R or X7R dielectric capacitors are recommended because of their excellent temperature stability and high pulse-current capability. If excessive circuit noise affects normal operation, the bypass capacitance may be increased to 50 to 100 times the equivalent load capacitance. Alternatively, the bypass network may be implemented using two parallel capacitors: one larger capacitor selected according to the equivalent load capacitance, and one smaller capacitor (typically 1 nF to 10 nF) placed as close as possible to the V_{CC} and GND pins to provide a low-impedance path for high-frequency current pulses.

Layout and connection guidelines

The AG27524 family of gate drivers incorporates fast reacting input circuits, shortage propagation delays, and powerful output stages capable of delivering current peaks over 5A to facilitate voltage transition times from under 10ns to over 150ns. The following layout and connection guidelines are strongly recommended:

Keep high current output and power ground paths separate logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL-level logic thresholds at driver inputs and enable pins.

- If the inputs to a channel are not externally connected, the internal 400kohm resistor indicated on block diagrams command a low output. In noisy environments, it may be necessary to tie inputs of an unused channel to VDD or GND using short traces to prevent noise from causing spurious output switching.
- Many high-speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re-triggering. These effects can be obvious if the circuit is tested in breadboarding or non-optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The AG27524 is compatible with many other industry standard drivers. In single input parts with enable pins, there is an internal 400kohm resistor tied to VDD to enable the driver by default, this should be considered in the PCB layout.
- The turn on and turn off current paths should be minimized, as discussed in the following section The figure below shows the pulsed gate drive current path when the gate driver is supplying gate charge to

turn the MOSFET on. The current is supplied from the local bypass capacitor, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized bypass capacitor acts to contain the high peak current pulses within this driver MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

Fig 7. Current path for MOSFET turns on

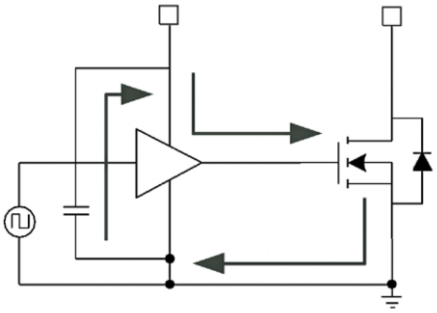
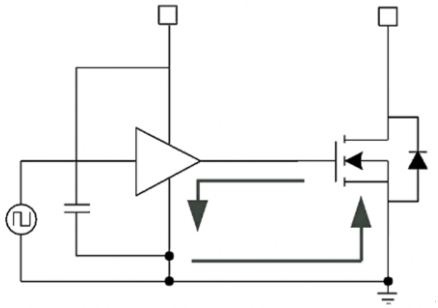


Fig 8. Current path for MOSFET turns off



The figure below shows the current path when the gate driver turns the MOSFET off. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn off times, the resistance and inductance in this path should be minimized.

Truth table of logic operation

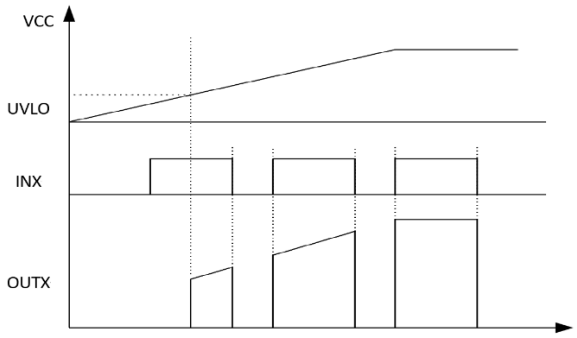
The AG27524 truth table indicates the operational states using the dual input configuration. If the INA/INB pins are connected to logic high, a disabled function is realized, and the driver output remains LOW regardless of the state of the INA/INB pins.

INA/INB	ENA/ENB	V_{CC}	OUTA/B
1	1	>UVLO	1
0	1	>UVLO	0
X	0	>UVLO	0
X	X	<UVLO	0

Operational waveforms

At power up, the driver output remains LOW until the V_{CC} voltage reaches the turn on threshold. The magnitude of the output pulsed rises with V_{CC} until steady state V_{CC} is reached. The operation illustrated in the figure below shows that the output remains LOW until the UVLO threshold is reached, then the output is in phase with the input.

Fig 9. The AG27524 start-up waveform



Thermal Guidelines

Gate drivers used to switch MOSFETs, IGBTs and GaNs or SiCs at high frequencies can dissipate significant amounts of power. It is important to determine the drive power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits. The total power dissipation in gate driver is the sum of two components, Gate Driving Loss and Dynamic Power Loss. Gate driving loss PGATE is the most significant power loss result from suppling gate current to switch the load on and off at the switching frequency. The power dissipation that results from driving a power switch at a special gate-source voltage, VGS, with gate charge, QG, at switching frequency, FSW, is determined by:

P_{GATE}=n x Q_G x V_{GS} x F_{SW}

Where n is the number of driver channels in use (1 or 2). Dynamic power loss PDYN is the power loss resulting from internal current consumption under dynamic operating conditions, including pin pull-up / pull-down resistor. The internal current consumption IDYN can be estimated using the graphs of the typical performance characteristics to determine the current IDYN drawn from V_{CC} under actual operating conditions:

P_{DYN}=V_{CC} x I_{DYN} x m

Where m is the number of driver ICs in use. Note that m is usually one IC even if in parallel to drive a large load. Once the power dissipation in the driver is determined, the driver junction rises with respect to circuit board can be evaluated using the following thermal equation, assuming JB Ψwas determined for a similar thermal design:

$$T_J = (P_{GATE} + P_{DYN}) \times \Psi_{JB} + T_{BOARD}$$

Where TJ is the driver junction temperature; ΨJB is thermal characterization parameter relating temperature rise to total power dissipation;

TBOARD is the board temperature in location as defined in the thermal characteristics table.

To give a numerical example, assume for a 12V V_{CC} system, the power MOSFETs which have a total gate charge of 60nC at VGS=12V. Therefore, two devices in parallel would have 120nC gate charge. At a switching frequency of 200kHz, the total power dissipation is:

P_{GATE}= 2 x 120nC x 12kHz = 0.576W

P_{DYN}= 12V x 1.4mA x 1 = 0.0168W

P_{TOTAL}= P_{GATE} + P_{DYN} = 0.593W

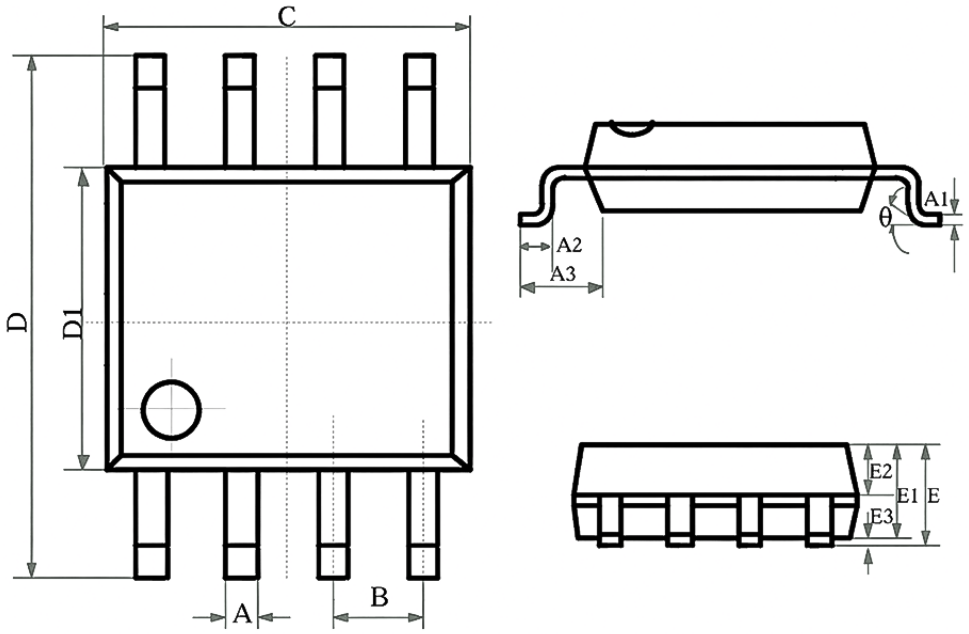
The SOP8 has a junction to board thermal characterization parameter of ΨJB =42℃/W. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must be prevented from exceeding the maximum rating of 150℃, with 80% derating, TJ would be limited to 120℃. Rearranging equation TJ determines the board temperature required to maintain the junction temperature below 120℃.

$T_{BOARDMAX}$=TJ – ΨJB x P_{TOTAL}

$T_{BOARDMAX}$=120℃ - 42℃/W x 0.593 =95℃

PACKAGE INFORMATION

Dimension in SOP8 (Unit: mm)



Symbol	Min.	Max.
A	0.39-	0.480
A1	0.210	0.280
A2	0.500	0.800
A3	1.050 BSC.	
B	1.270 BSC.	
C	4.700	5.100
D	5.800	6.200
D1	3.700	4.100
E	-	1.750
E1	1.300	1.500
E2	0.600	0.700
E3	0.100	0.225
θ	0°	8°

IMPORTANT NOTICE

AiT Semiconductor Inc. (AiT) reserves the right to make changes to any of its products, specifications, to discontinue any integrated circuit product or service without notice and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

AiT Semiconductor Inc.'s integrated circuit products are not designed, intended, authorized, or warranted to be suitable for use in life support applications, devices or systems or other critical applications. Use of AiT products in such applications is understood to be fully at risk of the customer. As used herein may involve potential risks of death, personal injury, or server property, or environmental damage. In order to minimize risks associated with the customer's applications, the customer should provide adequate design and operating safeguards.

AiT Semiconductor Inc. assumes to no liability to customer product design or application support. AiT warrants the performance of its products of the specifications applicable at the time of sale.